TELEDYNE LECROY
Everywhereyoulook™

Summit™ M64 Protocol Analyzer and Exerciser

for PCIe® 6.x, NVMe and Compute Express Link™

Key Features

Find errors fast
- One button error check
- Fast upload speed
- Large trace memory
- Powerful triggering/filtering

See and understand the traffic
- Get useful information
- More choices of data views
- More ways to analyze data
- Custom decoding and reports

Data capture
- 100% data capture at 64.0 GT/s on all link widths up to x4

Deep memory buffer
- Up to 32 GB depth

PCIe storage protocols supported
- NVM Express
- NVMe-MI
- SATA Express (ATA/AHCI-PCIe)
- SCSI Express (SOP-PQI)

Virtualization protocols
- SRIOV
- MRIOV
- ATS

Sideband signaling
- SMBus
- CLKREQ#
- WAKE#
- PERST#

Supports CXL
- Supports all three CXL sub-protocols and all CXL device types

Supports Lane Margining

Supports MultiPort™ analysis

Supports PCIe IDE/DOE

Supports CXL IDE

The Summit M64 offers advanced features such as: support for PCI Express 6.x, NVMe® and CXL™ Specification; data rates of 2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, 32.0 GT/s, and 64.0 GT/s; full data capture on bidirectional link widths of x1, x2, and x4; and up to 32 GB of trace memory. The product is ideal for high-performance protocol development for add-in boards, servers and workstations, and for customers currently working on CXL, PCIe® 6.x.

Advanced Protocol Analysis

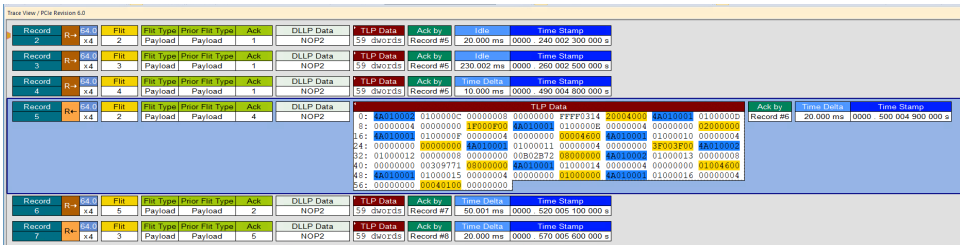
The Summit M64 protocol analyzer features support for the PCIe 6.x technology at speeds of up to 64.0 GT/s and up to x4 link widths. It also provides up to 32 GB of trace memory recording capability. The Summit M64 can be controlled through USB or can be remotely networked and controlled through a 1000baseT Ethernet connection. It can also be synchronized with other high-speed protocol analyzers or oscilloscopes from Teledyne LeCroy.

The Summit M64 is also a fully featured Protocol Analyzer for Compute Express Link (CXL). Support is provided for CXL.io, CXL. mem and CXL.cache with full decoding from the FLIT layer to the CXL link and transaction layers.

Capturing is performed by connecting a PCIe 6.0 interposer or probe between the Host System/ Root Complex and the Device Under Test (DUT). Interposers and probes are offered in various link widths.

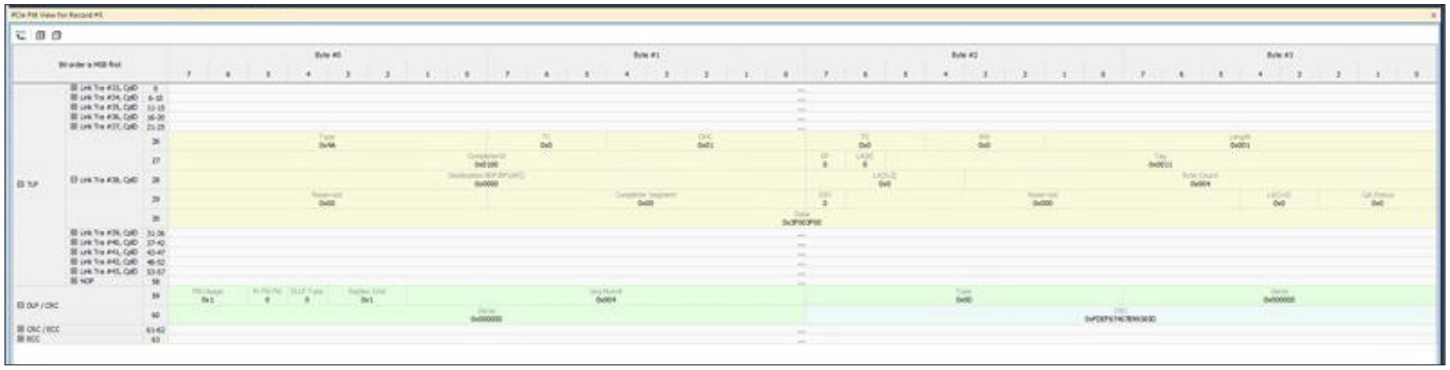
The Summit M64 for PCI Express 6.x and CXL provides multiple views including: CATC Trace™; Spreadsheet View; LTSSM State View; and other focused views to assist users in analyzing how PCI Express protocol components work together, facilitating more effective problem diagnosis. These various interfaces help find errors fast by utilizing precise triggering, filtering and error reporting. Together they compose a powerful and intuitive expert software system, embedding detailed knowledge of the intricacies of the protocol hierarchy as defined in the specification.

Graphical displays have been optimized for fast and easy navigation. Users are alerted as violations are detected at all layers of the protocol and can easily drill down into areas of interest. Users can also quickly and easily collapse and/or hide fields that are not relevant. Protocol data can be viewed in several ways from logical to chronological, and by events unique to PCI Express or CXL.



PCI Express 6.x trace describing Flit mode details

All Teledyne LeCroy PCI Express and CXL protocol analyzers feature a hierarchical display of protocol traffic summaries, detailed error reports, powerful scripting, and the ability to create user-defined test reports, which allow developers to troubleshoot intricate problems and finish their projects on time.



PCI Express 6.x Register View describing Flit fields

Integrated Exerciser

The Summit M64 exerciser is designed for developers who need a protocol test system supporting the PCI Express® 6.x and CXL specifications. Supporting traffic generation at data rates to 64.0 GT/s with link widths up to 4 lanes, the Summit M64 is Teledyne LeCroy's latest PCI Express (PCIe®) protocol exerciser, leveraging years of experience in providing advanced protocol test and compliance tools to the PCI Express community.

The Summit M64 exerciser supports full traffic generation and device/ host emulation, and provides the industry a platform for development of standardized compliance test suites. In addition, the system provides error injection functions to enable developers to test error recovery routines important to reliable interoperability of PCI Express 6.x and CXL products.

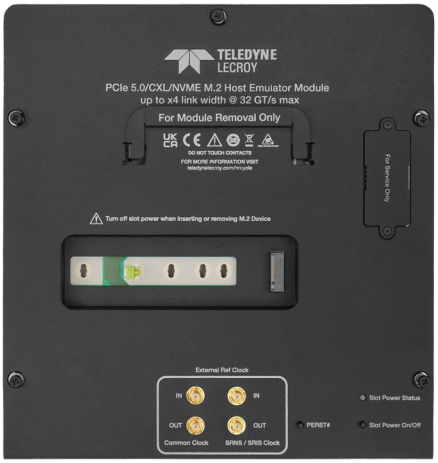
PCIe Exerciser

- Error injection
- Provides traffic generation and host/device emulation
- Supports NVMe/NVMe-MI
- Emulate root complexes or device endpoints
- Exercise LTSSM state transitions
- Generate controlled error conditions to test error recovery routines
- Supports Exercising SMBus, MCTP
- Supports Exercising Sideband Signals
- Can be used in Common Clock and SRIS environments
- Supports Alternate Protocol

Three Host Emulator Modules are available for CEM, EDSFF and M.2 emulation.

Summit M64 Protocol Exerciser
Host Emulator CEM Module

Summit M64 Protocol Exerciser
Host Emulator EDSFF Module



Summit M64 Protocol Exerciser
Host Emulator M.2 Module

Typical Applications

The Summit M64 exerciser is a critical test and verification tool to assist engineers in development, debug and validation of their PCIe and CXL designs (including early stage power-on testing). Because of its rich programmable environment, scripting can be employed for full interoperability testing to improve the reliability of systems.

The Summit M64 exerciser can emulate either PCIe and CXL root complexes or device endpoints, allowing new designs to be tested against known standards.

A Wealth of PCI Express Features

An intuitive software interface allows the user to create sophisticated traffic patterns, and when combined with a protocol analyzer, test suites can be rapidly customized to meet the user's specific requirements. One feature that helps troubleshoot PCIe-based links is the ability to fully exercise the Link Training and Status State Machine (LTSSM) transitions.

Powerful scripting language also allows for the creation of Transaction Layer Packets (TLPs) and Data Link Layer Packets (DLLPs) at PCIe 6.x data rates of 64.0 GT/s. Flow Control and ACK/NAK's policies and structures can be defined and generated under user control.

Features addressing LTSSM structures include providing bus traffic to emulate all the states of the LTSSM from the Detect state, to the L0 state and maintaining the L0 state between the host and device. The exerciser also supports lane reversal and can control all polarity and scrambling configurations. An important feature to note is that traffic emulation supports dynamic equalization in addition to skipping the EQ phases entirely. The exerciser also has the capability to perform error injection for training sequences, as well as Data Link and Transaction Layer traffic, both at the packet level and on a per lane basis.

Packet fields not explicitly specified by the user are generated automatically (such as packet numbering and CRCs). The configuration space can be emulated for any device including endpoints, bridges and switches. Support for all PCIe 6.0 data rates allows the Summit M64 to produce test cases that test the device's ability to auto- negotiate data rates with other devices.

In addition, the ability of the Summit M64 to produce a wide variety of programmed traffic allows the user to introduce controlled error conditions. As an example, a trace file captured by the external Summit series PCIe protocol analyzer can be exported and used as the basis for a test script, with selected programmed errors introduced at critical stages to test the device's ability to recognize and recover from error conditions. This allows for detailed testing of simple error recovery and complex multiple error conditions, creating more resilient products that perform well even under less than ideal conditions.

TAP^6 TECHNOLOGY

What is TAP^6 technology and what is it for?

TAP^6 is Teledyne LeCroy's latest generation custom probing silicon designed specifically to "de-embed" Teledyne LeCroy's probes from the DUT. TAP^6 employs a combination of signal splitters and linear amplifiers along with highly configurable DFE and CTLE adaptive equalizers to remove the effects of the probe from the active circuit.

TAP^6 circuitry has been so designed to provide as flat a response as possible over a very broad range of frequencies that are targeted to align with the needs of the PCIe specification, up to and beyond the current PCIe 6.x specification.

What are the benefits of using Teledyne LeCroy's TAP^6 technology

TAP^6 based probes and interposers can easily operate in a "plug and play" manner using its default values when used in environments that fully meet the PCIe specification.

When used in less than ideal environments or with early prototypes that may still be in design and /or operate marginally, the TAP^6 based probe can be adjusted to compensate for signaling limitations causing operating issues on the channel.

Full CXL Traffic Generation and Error Insertion Capabilities

Compute Express Link (CXL) is a high-speed CPU-to-Device and CPU-to-Memory interconnect designed to accelerate next-generation data center performance. CXL is based on the PCI Express 6x Physical layer with speeds up to 64.0 GT/s. The exerciser scripting language also allows for the creation of CXL Transaction Layer Packets (CXL.io TLPs) and Data Link Layer Packets (CXL.io DLLPs) in addition to CXL.mem and CXL.cache requests at PCIe 6.x data rates of up to 64.0 GT/s. Flow Control and acknowledge policies and Flit structures for each of the CXL protocols: CXL.io, CXL.mem, CXL.cache can be defined and generated under user control.

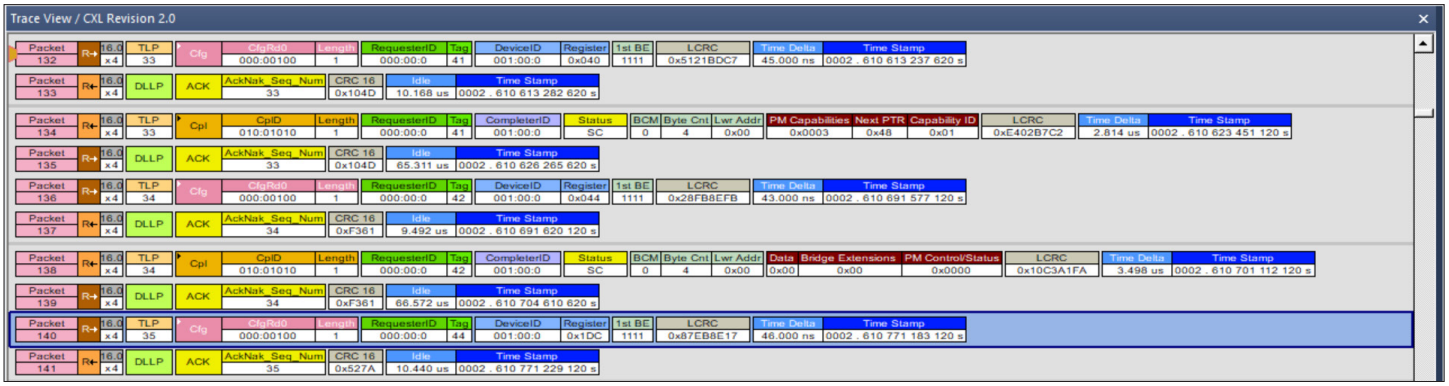
The Summit M64 can also generate CXL.io, CXL.cache, and CXL.mem packets that can be dynamically multiplexed on the link. It can provide traffic and error generation for systems through all layers from the FlexBus Physical layer and Flits all the way up to the Link and Transaction Layers.

Users of Teledyne LeCroy systems appreciate the rich library of decodes and analysis capabilities that are available on all of Teledyne LeCroy's PCIe test tools.

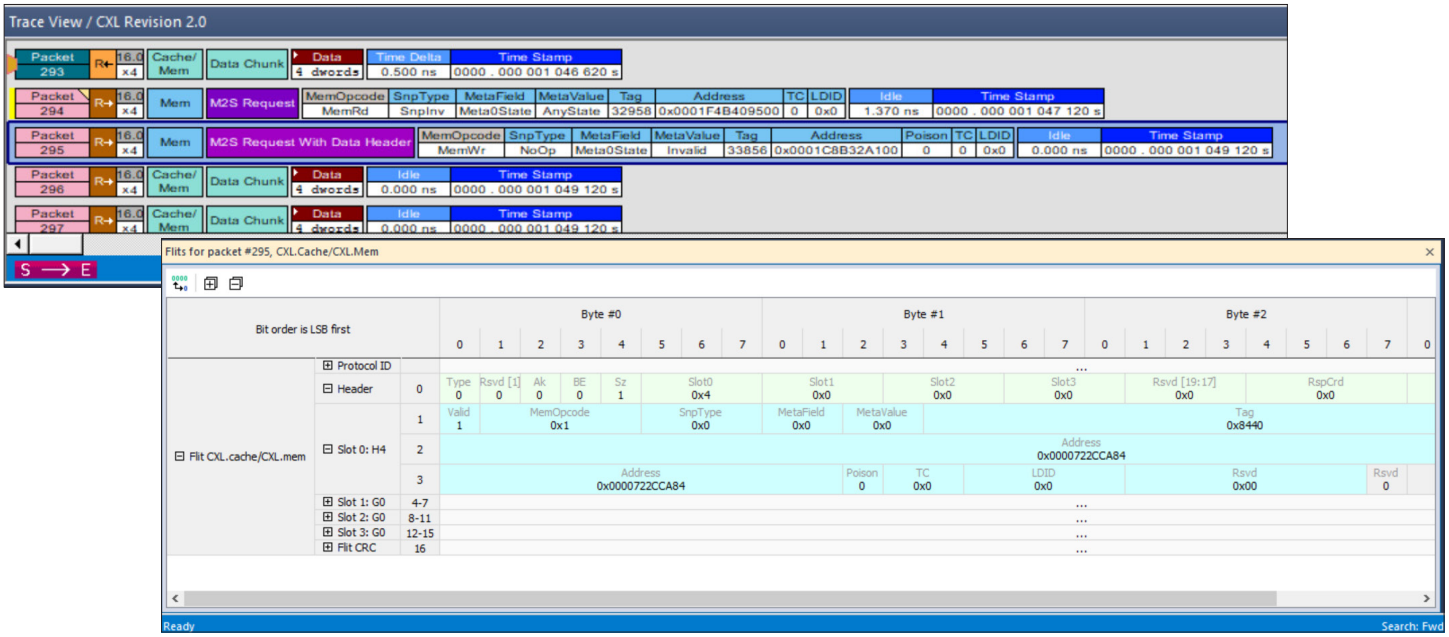
The Summit M64 offers extensive decoding for Storage protocols like NVM Express® and SATA Express®. DataCenter monitoring technology such as NVMe® queue characterization, NVMe-MI™ and out-of-band SMBus signaling which is decoded and synchronized with PCI Express can be analyzed for protocol traffic issues. If IO virtualization is important SRIOV and MRIOV is also decoded and analyzed.

CXL Features

- Supports all three CXL device types
- Generates ALMP requests
- Emulates CXL Hosts and Devices
- Supports normal and degraded modes



CXL trace showing ACKs and completions



CXL Register View showing CXL.Cache and CXL.Mem fields

Specifications	
Host Machine Minimum Requirements	64-bit (x64) versions of Windows® 11, Windows 10, Windows Server 2016, and Windows Server 2019. o The latest Service Pack available for the Windows OS in use is required. 4 GB of RAM; storage with at least 2 GB of free space for the installation of the software and additional space for recorded data; display with resolution of at least 1024x768 with at least 16-bit color depth; USB 2.0/3.0/3.1 port and/ or 100/1000 Mbps Ethernet network interface. For optimal performance, please refer to our recommended configuration in the product documentation.
Data Rates Supported	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, 32.0 GT/s and 64.0 GT/s (PCI Express® 6.x)
LEDs	Power LED, Status LED, Trigger LED, and lane LED for all 4 US lanes and 4 DS lanes
Dimensions and Weight	16.75" (425.45 mm) length x 17.00" (431.8 mm) width x 3.44" (87.4 mm) or (2U) height; 16lbs
Power Requirements	90 - 264 VAC, 47 - 63 Hz, 0 - 264 VAC, 47 - 63 Hz, 550W
Environmental	Temperature (operating): 5° to 40°C (41° to 104°F) Temperature (non-operating): -20° to 60°C (-4° to 140° F) Humidity (operating): 5% to 80% RH (non-condensing) at <=30°C, 50% max RH (non-condensing) at 40°C Humidity (non-operating): 5% to 95% max RH (non-condensing)
Recording Memory Size	Up to 32 GB
Ports	USB 3.0 Type C connector, Trigger in and out, GB/s ethernet port, Sync in/out expansion port
Switches/Buttons	Power Switch, Navigation Button

Additional Features

- ✓ Protocol Hierarchical Display
- ✓ Spreadsheet View
- ✓ Queue Utilization
- ✓ NVMe
- ✓ SATA Express
- ✓ NVMe-MI
- ✓ SMBus
- ✓ CXL Decoding
- ✓ ZeroTime™ Search
- ✓ Dword View
- ✓ LTSSM View
- ✓ Header Field Viewer
- ✓ Config Spec Viewer
- ✓ TLP Packet Script Decoding
- ✓ Timing Calculator
- ✓ Trigger/Filter Control
- ✓ Performance Metrics
- ✓ Expert Triggering
- ✓ Trace Expert
- ✓ Expert Graphical Bus Utilization View
- ✓ Verification Script Engine
- ✓ 1 GB/s Ethernet & USB 3.0
- ✓ TCG Decoding
- ✓ CrossSync PHY Capable
- ✓ Supports PCIe Integrity and Data Encryption (IDE)
- ✓ Supports CXL IDE

Ordering Information

Product Description	Product Code
Summit M64 (licensed as a Gen6 x4 analyzer at 16GB memory)	PE6600AAA-X
Summit M64 (licensed as a Gen5 x4 analyzer at 16GB memory)	PE6602AAA-X
Exerciser Host Emulator Modules	
Summit M64 Protocol Exerciser Host Emulator CEM Module	PE6601UEA-X
Summit M64 Protocol Exerciser Host Emulator EDSFF Module	PE6602UEA-X
Summit M64 Protocol Exerciser Host Emulator M.2 Module	PE6603UEA-X

Local sales offices are located throughout the world.
Visit our website to find the most convenient location.

1-800-5-LeCroy • teledynelecroy.com

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