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HIRATE – HIGH PERFORMANCE DIGITAL RADIO TESTBED

AT A GLANCE

- Highly flexible modular testbed comprising digital baseband platform and plug-on modules
- SISO and 2×2 MIMO capabilities
- 250 MHz system bandwidth
- Easy-to-use GUI-based control
- Design flow for high level FPGA development based on Altera DSP Builder®
- Hardware-in-the-loop operation mode with MATLAB® interface
- Various plug-on modules available, custom designs by user or vendor
- Compact 19“ chassis

Features

- Two complete Tx and Rx chains
- FDD and TDD operation
- Adaptable frequency range
- Synchronization and coherent operation capability of multiple HIRATE devices
- Simultaneous real-time and hard-ware-in-the-loop operation
- Development of digital signal processing algorithms by user or vendor (HIL and real-time)

Applications

- Indoor/outdoor wireless transmission experiments
- Waveform generation and analysis
- Wideband RF impairment compensation – power amplifier linearization and IQ-imbalance compensation
- Wideband MIMO channel sounding
- University teaching

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Digital Signal Processing and System Control

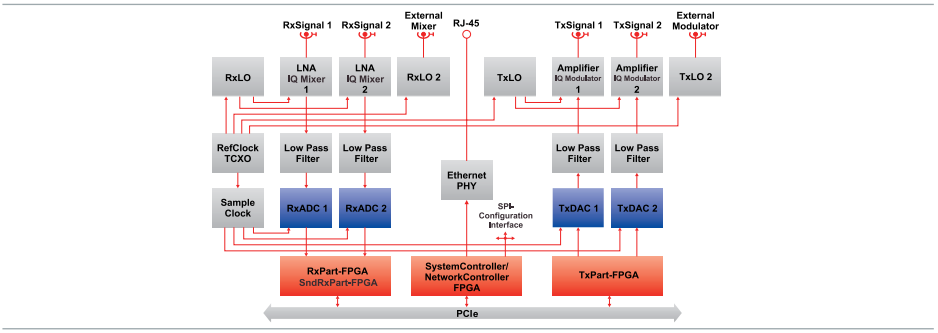
- 4×Altera® Stratix® III FPGAs
- Embedded microcontrollers for application control and network protocol processing
- 110K/260K logic elements (standard/extended HIRATE configuration)

Signal Conversion

- Two IQ Tx DACs with 16 bit, 250 MSps (internal: 500 MSps), SFDR: 82 dBc, DNL: 2.1 LSB, INL: 3.7 LSB
- Two IQ Rx DACs with 8 bit, 500 Msps, SNR: 45 dB, SFDR: 54 dBc, ENOB: 7.2
- On-board signal memory: 8 MS per channel at Tx, 16 MS/channel at Rx

External Interfaces

- PCI Express host interface, up to 4 lanes, max. throughput approx. 500 MBps, cable length up to 7 m



HIRATE system architecture

- Gigabit Ethernet, RJ45 connector
- 8 SMA connectors for analog/RF signals: transmit and receive signals, LO, reference
- JTAG interface for embedded processor debugging
- Logic analyzer interface (optional)

Software

- Operational software available for Microsoft Windows® operating systems
- Graphical user interface (GUI) for system control
- Predefined MATLAB® functions and scripts for hardware-in-the-loop operation
- Design flow for high level FPGA development based on Altera® DSP Builder®
- Several IP cores available for real-time implementations

General Specifications

- Power supply: 100 to 240 VAC, 50 Hz to 60 Hz
- Power consumption: 30 W to 90 W (application-specific), standby < 1 W
- Operating temperature range: 10°C to 50°C
- 19" chassis: 3U height, 410 mm depth

The Fraunhofer HHI

One of the prime research and development foci of the Fraunhofer Heinrich Hertz Institute lies in the development of mobile and fixed broadband communication networks and multimedia systems.

Contact

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