ADSANTEC
Ultra High-Speed Mixed Signal ASICs
Advanced Science And Novel Technology Company, Inc.
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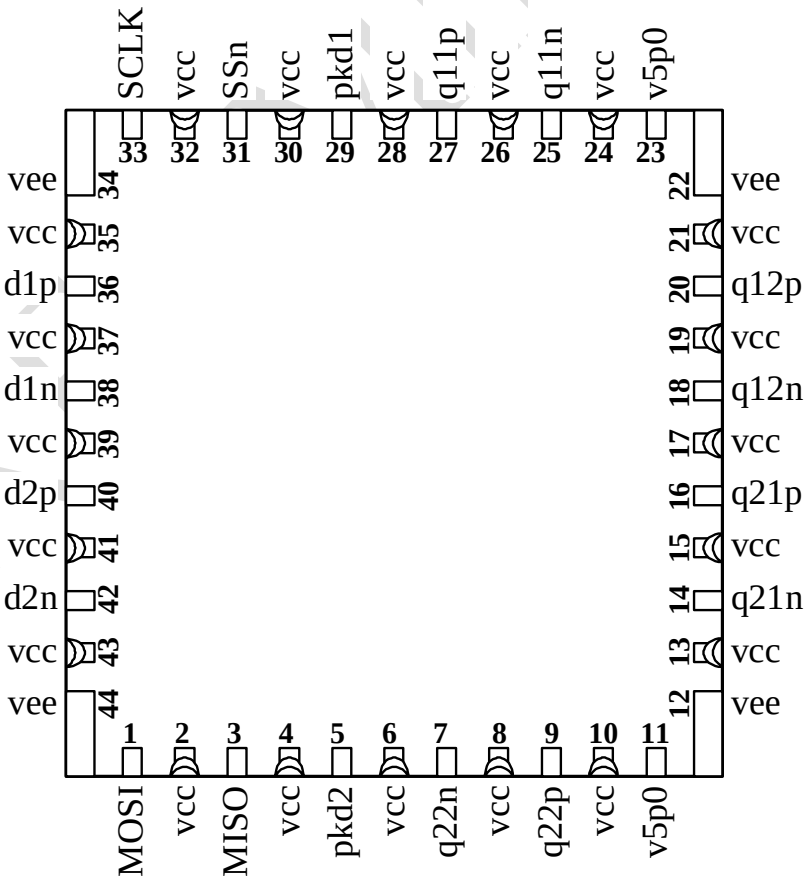
Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ASNT6153-KHM
Dual 2-Channel CTLE with Peak Detectors

- High-speed adjustable linear equalizer
- Two independent data channels with two independent equalization paths per channel
- Independently adjustable 5 zeros and 2 poles in each path AC response
- Independent gain adjustment in each equalization path
- High-speed CMOS 3-wire interface for chip control
- Input peak detectors in both channels
- Fully differential CML-type analog input and output interfaces
- Two power supplies for the data paths and AC control circuitry
- Average power consumption: 1.4*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Limited temperature variation over industrial temperature range
- Die size 1.5x1.5mm^2
- Custom CQFN 44-pin package



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DESCRIPTION

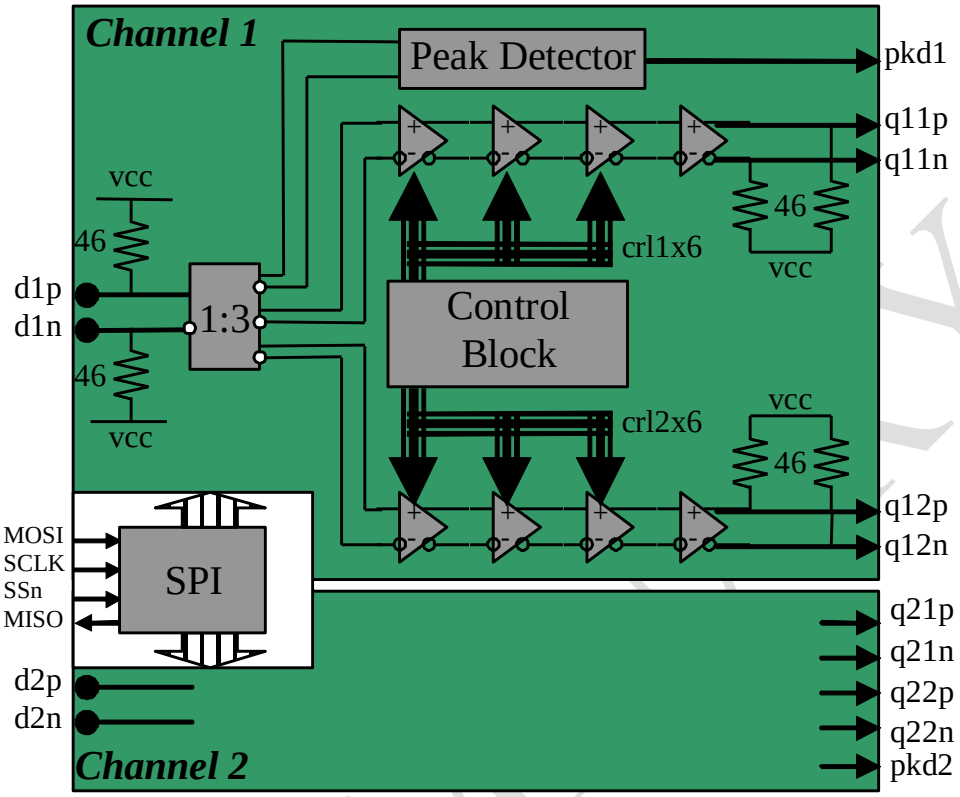


Fig. 1. Functional Block Diagram

The IC shown in Fig. 1 is a two-channel adjustable continuous-time linear equalizer (CTLE) with two independently controlled analog data equalization paths per channel. Each equalization path has its own output. The AC response of each path has 6 controls: adjustable DC gain, 3 independently adjustable zeros, and 2 independently adjustable poles.

Input Peak Detectors that represent the input signal amplitude are added to each channel.

The part's I/Os support CML-type differential interface with on-chip 46*Ohm* termination to vcc. Matching external terminations are also required.

All operational modes of the chip are controlled by a Control Block that communicates with an external computer through a high-speed 3-wire serial interface.

The part operates with a positive supply vcc = +3.3*V* for the main data paths, and an additional positive supply v5p0 = +5.0*V* for the AC control circuitry. The negative supply rail vee should be connected to external ground as shown in Fig. 2a.

The part can also operate with a negative supply vee = -3.3*V* for the main data paths, and an additional positive supply v5p0 = +1.7*V* for the AC control circuitry. In this case the positive

supply rail vcc should be connected to external ground as shown in Fig. 2b. Also, the SPI input and output signals should be connected through DC blocks, or optocouplers.

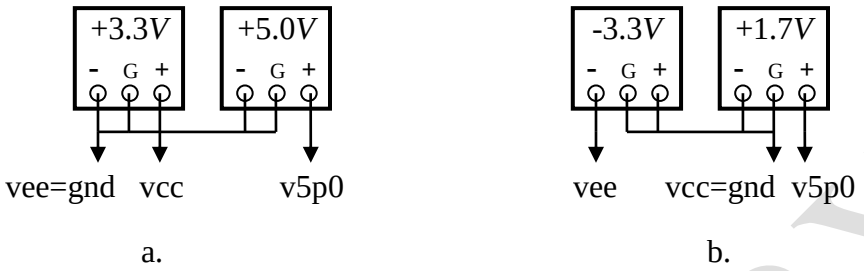


Fig. 2. Power Supply Configurations: Positive (a) and Negative (b)

Equalization Path

Typical AC responses of an Equalization Path are shown in Fig. 3.

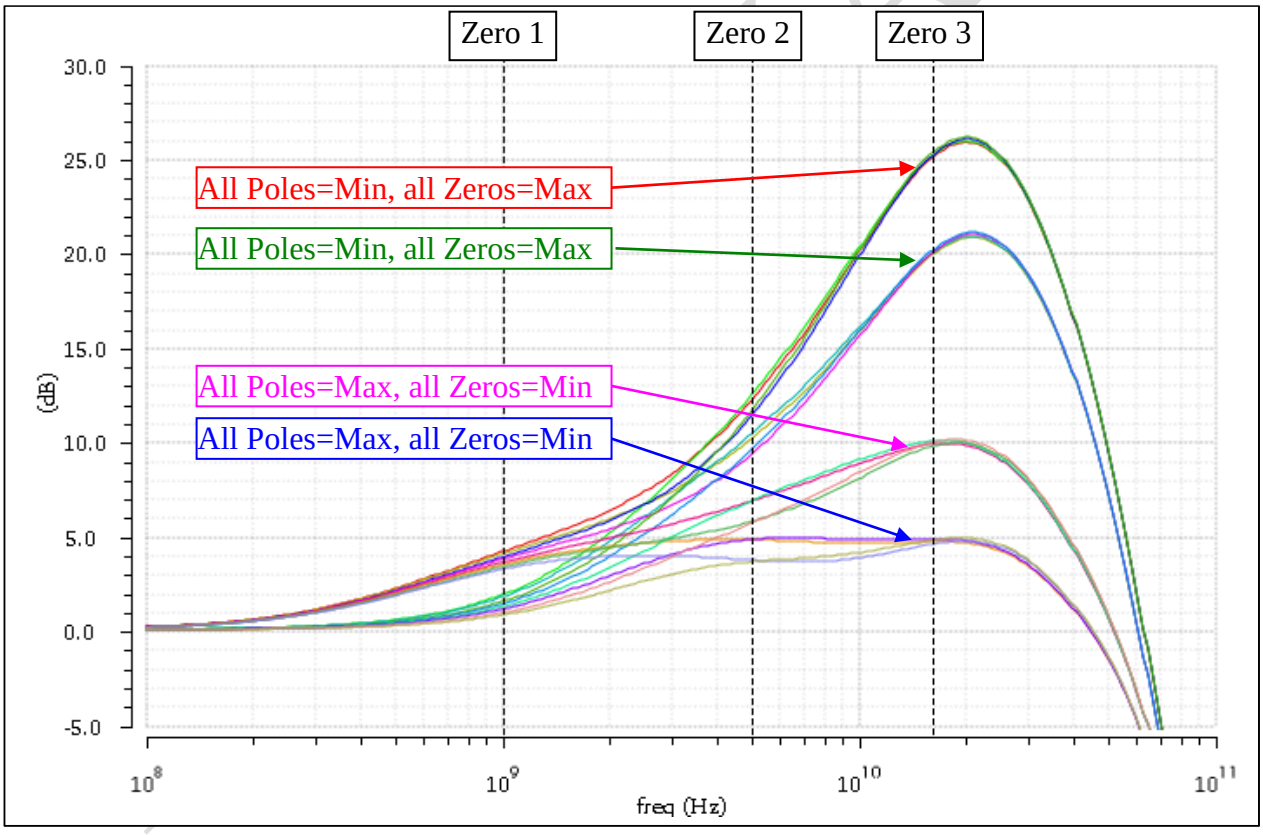


Fig. 3. Typical AC responses of an Equalization Path

Each path has 3 independent adjustable Zeros, and two independent adjustable Poles. For each setting, the DC gain can be adjusted between -3dB and +5dB.

Additionally, the path's bandwidth (BW) can be also adjusted as shown by the red and magenta curves in Fig. 4 that are plotted for the Max Pole, and Min Zero setting.

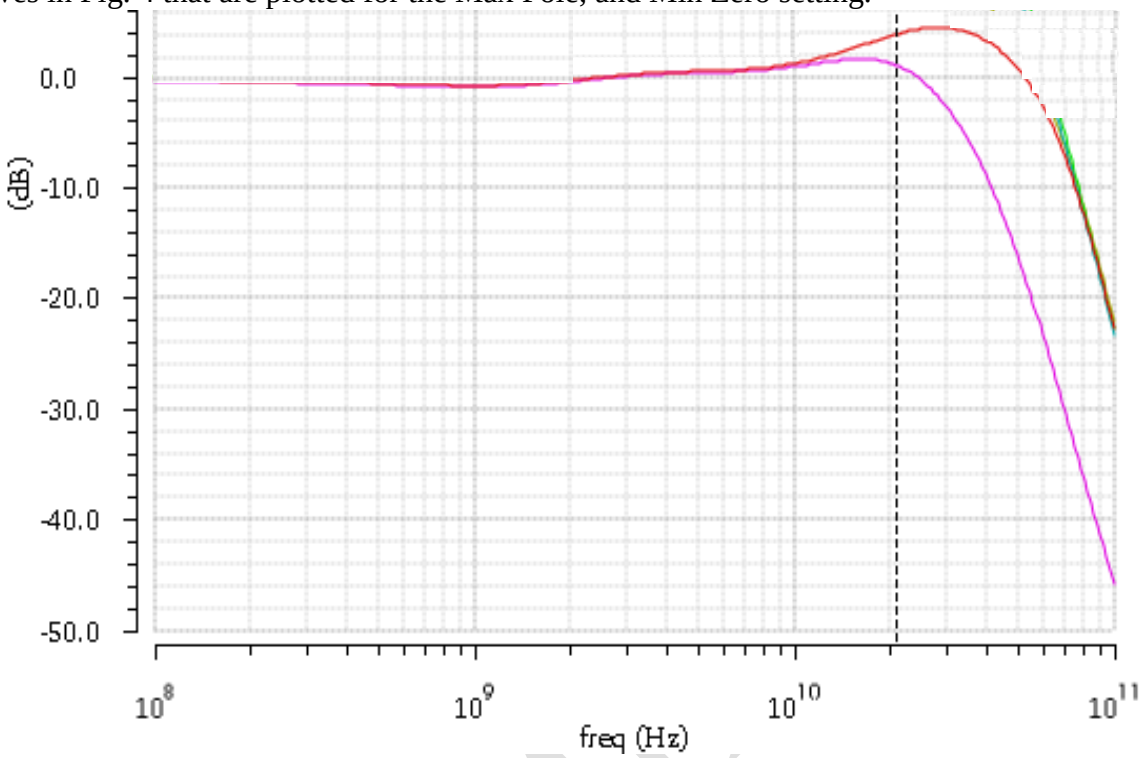


Fig. 4. DC Gain and BW Control Characteristics

Peak Detector

The Peak Detector block represents the single-ended swing of its input signal as an output voltage between 1.65*V* to 2.85*V*. The typical characteristics for a 1*GHz* sinusoidal input signal at different PT operational conditions are shown in Fig. 5.

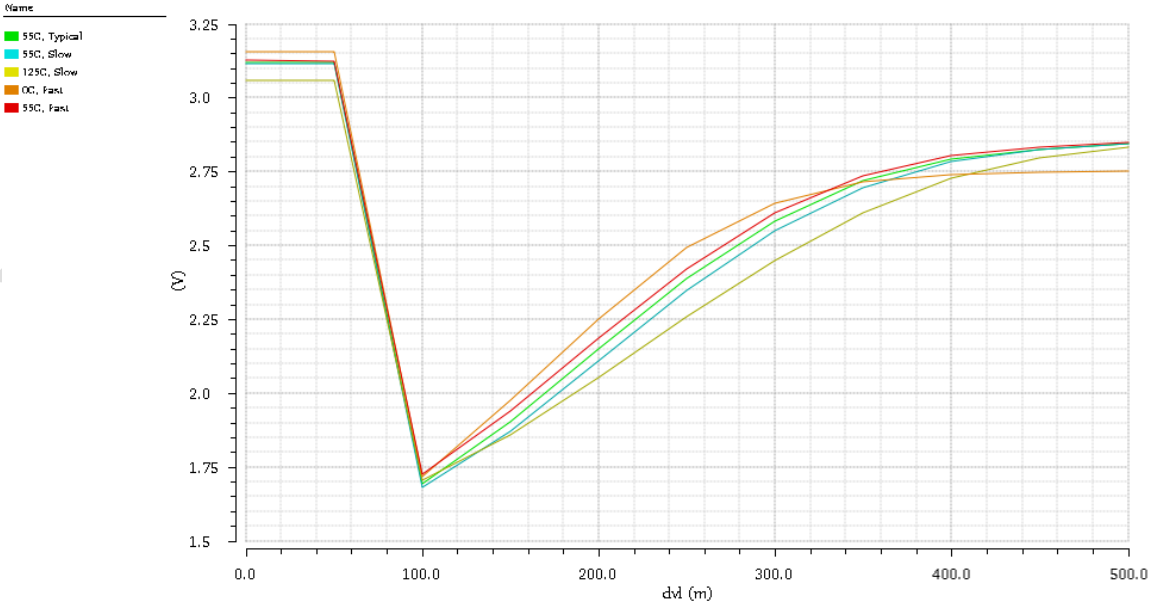
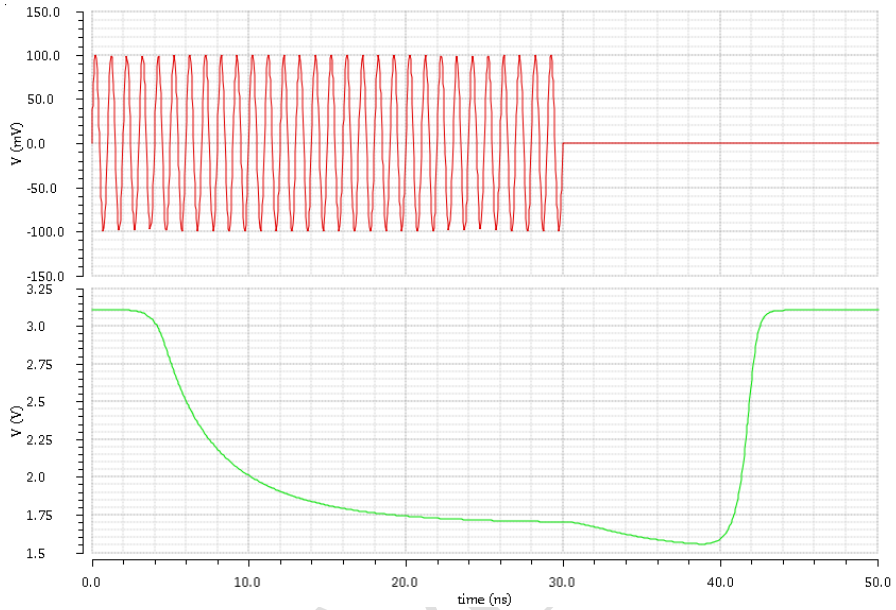


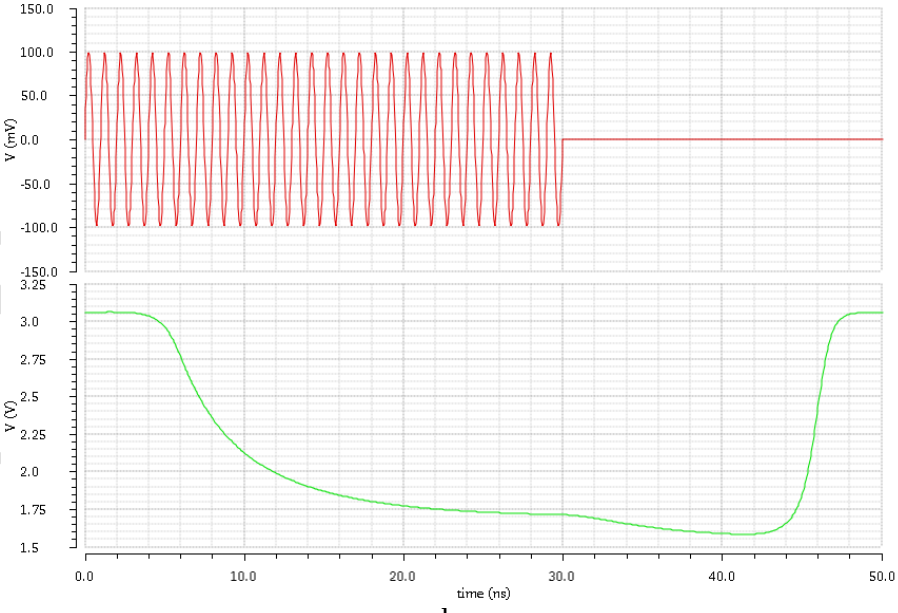
Fig. 5. Peak Detector Typical Simulated Characteristics for Different T° and Process Corners

As can be seen in the plot, the signal swings below a certain value are represented by the high voltage above 3.0V. This function can be used as an indication of NO Input Signal (Loss-of-signal, or LOS). The LOS threshold can be adjusted as desired.

The Peak Detector features a short settling time as shown in Fig. 6 that shows the sinusoidal input signal, and the Peak Detector output at different operational conditions.



a.



b.

Fig. 6. Peak Detector settling Time (a – Nominal, b – Worst Case Slow)

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3-Wire Interface

All functions of the chip are controlled through a 3-wire SPI. The interface includes a 16-byte internal register, and operates with 3.3*V* CMOS signals. It provides control signals for any of 2 groups of channels: Group A (Channels 1 and 2), and Group B (Channels 3 and 4). Each group data can be loaded independently, and the active group is selected by bit1 of byte16 in each data packet. The bit map of the interface is shown in Table 1.

Table 1. 3-Wire Interface Bit Map

Byte #	Bit #	Bit order	Signal name	Default Value	Signal function
1	From 7	MSB	zcl1_1	10000000	
	to 0	LSB			
2	From 7	MSB	zcm1_1	10000000	
	to 0	LSB			
3	From 7	MSB	zch1_1	01000000	
	to 0	LSB			
4	From 7	MSB	gc_1	10000000	
	to 0	LSB			
5	From 7	MSB	pc1_1	10000000	
	to 0	LSB			
6	From 7	MSB	pc2_1	10000000	
	to 0	LSB			
7	From 7	MSB	efc1	10000000	
	to 0	LSB			
8	From 7	MSB	zcl1_2	10000000	
	to 0	LSB			
9	From 7	MSB	zcm1_2	10000000	
	to 0	LSB			
10	From 7	MSB	zch1_2	01000000	
	to 0	LSB			
11	From 7	MSB	gc_2	10000000	
	to 0	LSB			
12	From 7	MSB	pc1_2	10000000	
	to 0	LSB			
13	From 7	MSB	pc2_2	10000000	
	to 0	LSB			
14	From 7	MSB	efc2	10000000	
	to 0	LSB			
15	From 7	MSB	losth1	10000000	
	to 0	LSB			
16	From 7	MSB	efc12	100000	
	to 2	LSB			
	1		wraddr	0	“0” – write to Group A, “1” – write to Group B
	0		-	0	Constant “0”

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The initial registers of the SPI are preset to the above default states at the time of the chip power supply activation.

TERMINAL FUNCTIONS

TERMINAL			Description
Name	**No.**	**Type**	
High-Speed I/Os			
d1p	36	CML-type Analog Inputs	Differential high-speed channel 1 data inputs with internal SE 46Ohm termination to vcc
d1n	38		
d2p	40		Differential high-speed channel 2 data inputs with internal SE 46Ohm termination to vcc
d2n	42		
q11p	27	CML-type Analog Outputs	Differential high-speed channel 1 path 1 data outputs with internal SE 46Ohm termination to vcc
q11n	25		
q12p	20		Differential high-speed channel 1 path 2 data outputs with internal SE 46Ohm termination to vcc
q12n	18		
q21p	16		Differential high-speed channel 2 path 1 data outputs with internal SE 46Ohm termination to vcc
q21n	14		
q22p	9		Differential high-speed channel 2 path 2 data outputs with internal SE 46Ohm termination to vcc
q22n	7		
Low-Speed I/Os			
SSn	31	3.3*V* CMOS I/Os	3-wire interface enable input with internal 474KOhm pull-up to vcc
SCLK	33		3-wire interface clock input with internal 474KOhm pull-down to vee
MOSI	1		3-wire interface data input with internal 474KOhm pull-down to vee
MISO	3		3-wire interface data output
pkd1	29	CMOS Output	Error Detector output and below-threshold signal amplitude indicator, with internal 6*KOhm* SE termination to vcc
pkd2	5		

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
v5p0	+5.0*V* positive power supply Negative pin to vee	11, 23
vee	Ground	12, 22, 34, 44
vcc	+3.3*V* positive power supply Negative pin to vee	2, 4, 6, 8, 10, 13, 15, 17, 19, 21, 24, 26, 28, 30, 32, 35, 37, 39, 41, 43

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

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Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Main Supply Voltage (vcc)		3.6	*V*
Additional Supply Voltage (v5p0)		5.5	*V*
RF Input Voltage Swing (SE)		750	*mV*
Case Temperature		+85	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee		0.0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	vcc in relation to vee
v5p0	4.8	5.0	5.3	*V*	v5p0 in relation to vee
I_{v5p0}	8		35	*mA*	Depending on the state of SPI control bytes
I_{vcc}	300		600	*mA*	
Power Consumption	1.1	1.4	2.1	*W*	
vcc ramp speed			10	*ms*	For reliable SPI preset
Junction temperature	0	50	125	*°C*	
Data input (d1p/d1n, d2p/d2n)					
Data Rate	DC		32	*Gb/s*	
SE Swing (differential signal is applied)			300	*mV*	0.3% THD at 1*GHz*
			500	*mV*	0.9% THD at 1*GHz*
CM Level	vcc-Swing/2				for DC input termination
Data output (q11p/q11n, q12p/q12n, q21p/q21n, q22p/q22n)					
Max peaking frequency	16		24	*GHz*	
Gain from Input	-3		+5	*dB*	Depending on SPI settings
CM Level	vcc-0.35			*V*	for DC output termination
Peak Detector output (pkd1, pkd2)					
Voltage range	1.65		2.88	*V*	For input swing control
	3.05		3.25	*V*	For LOS operation
Settling time	15		20	*ns*	
3-Wire Interface Port					
Clock frequency	0.1		50	*MHz*	
Input low logic level	vee		vee+0.3	*V*	
Input high logic level	vcc-1.3		vcc	*V*	
Output low logic level	vee		vee+0.2	*V*	
Output high logic level	vcc-0.3		vcc	*V*	
Input current			9	*uA*	For each input

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PACKAGE INFORMATION

The chip die is housed in a custom, 44-pin CQFN package shown in Fig. 7. The package provides a center heat slug located on the back side of the package to be used for heat dissipation. ADSANTEC recommends using extreme caution when soldering this section to the board to avoid overheating. It should be connected to the vcc plain that is ground for the negative supply, or power for the positive supply.

The part's identification label is ASNT6153-KHM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

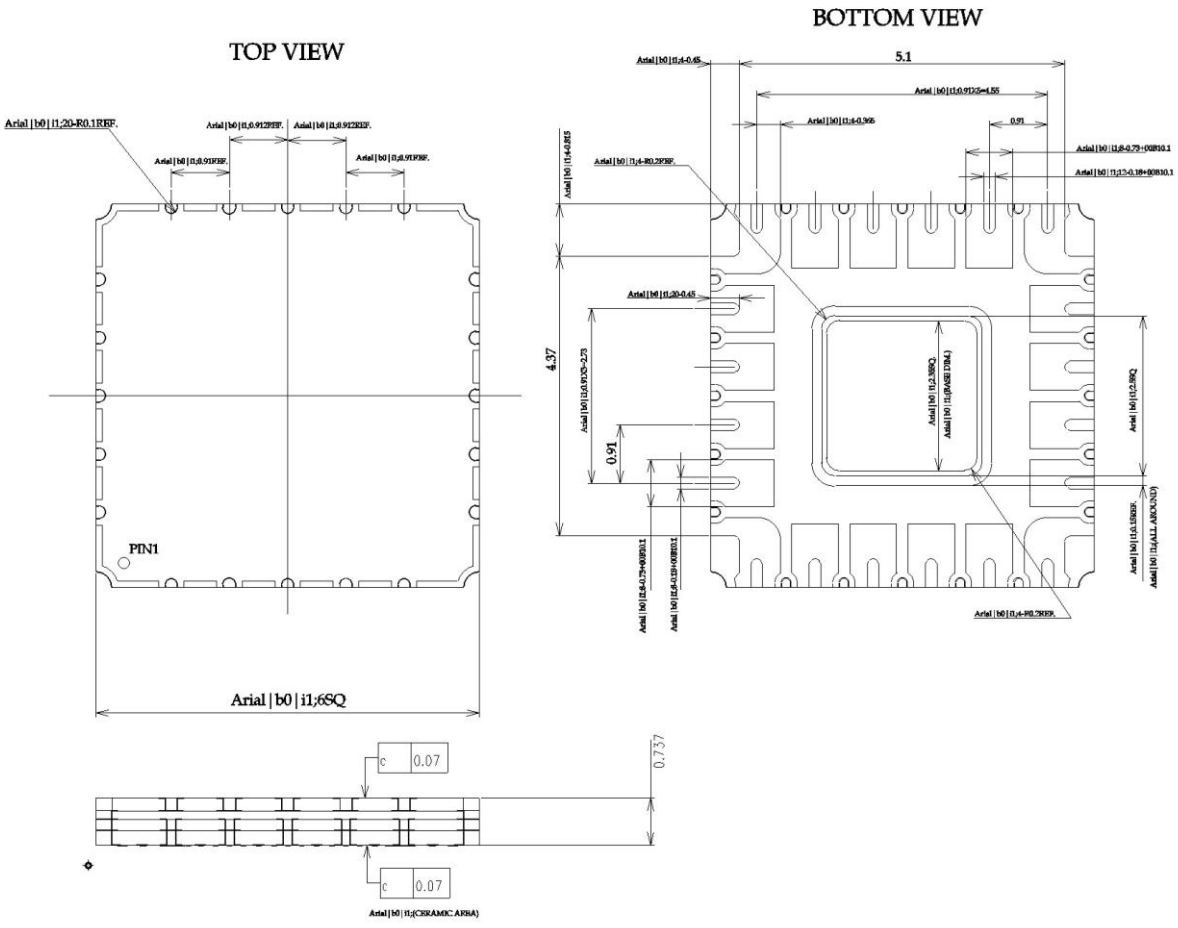

Fig. 7. CQFN44 Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
0.4.2	03-2021	Added power supply diagrams Changed recommendation for the package soldering
0.3.2	12-2020	Corrected temperature specifications
0.2.2	12-2020	Corrected Absolute Maximum RF swing Corrected pkd1/2 terminal description Corrected Electrical Specifications table
0.1.2	12-2020	Corrected SPI description
0.0.2	12-2020	Preliminary release