ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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ASNT MUX64
64*Gbps* 2:1 Multiplexer Unit

- High speed broadband 2-to-1 Multiplexer (MUX)
- Fully differential CML data input and output interfaces
- Single-ended CML clock input and output interfaces
- NRZ multiplexing and PAM4 generation support
- Built-in half-rate input clock phase shift capability
- Two single ended quarter-rate CML clock outputs with delay adjustment to support PAM4 signal generation (requires two MUX64 units)
- Full functional control from an external PC with a special GUI software (installation provided)
- USB port for connection to an external PC (PC not provided)
- Single 9*V* power supply from an external AC-DC converter (provided)
- Low jitter and limited temperature variation over industrial temperature range

Fig. 1. Front and back views of the unit

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DESCRIPTION

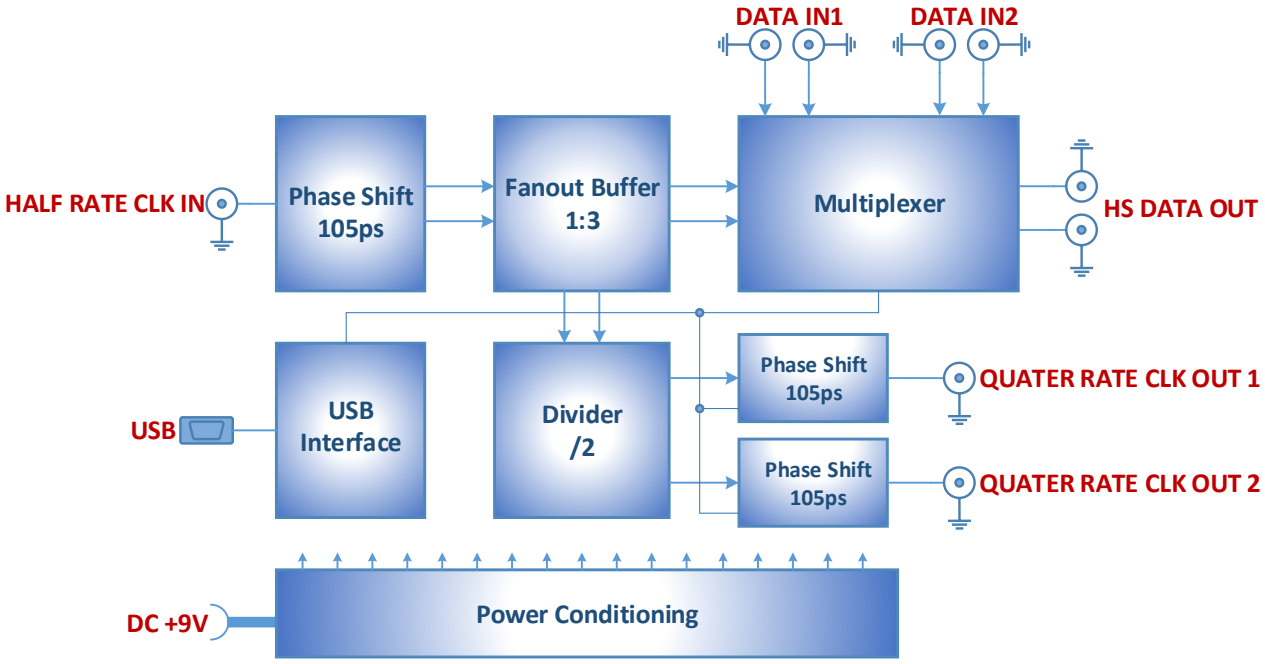

Fig. 2. Block diagram

The ASNT_MUX64 can be used for test applications, design verification, and R&D environments including double frequency rate NRZ data multiplexing and PAM4 generation, which requires two MUX units. The front panel of the instrument is shown in Fig. 1 (top). It includes connectors as described in Table 1.

Table 1. Front-panel connectors

Connector		DESCRIPTION
Name	Type	
High-Speed I/Os		
DATA OUT P	1.85*mm* female	DC-coupled CML differential data output port, requires external SE 50*Ohm* terminations to ground
DATA OUT N		
DATA IN1 P	2.92*mm* female	DC-coupled CML differential data input port with internal SE 50*Ohm* terminations to ground
DATA IN1 N		
DATA IN2 P		DC-coupled CML differential data input port with internal SE 50*Ohm* terminations to ground
DATA IN2 N		
CLOCK IN P		AC-coupled CML SE clock input port with internal SE 50*Ohm* terminations to ground
CLOCK ½ OUT Q1	SMA	AC-coupled CML SE clock output ports, require external SE 50*Ohm* terminations to ground
CLOCK ½ OUT Q2		

The back panel of the instrument is shown in Fig. 1 (bottom). It contains a power switch (Power), a power supply female connector (+9-12*V* DC) for connecting a male 2.5x5.5 barrel jack of the external AC-DC adapter, and the USB-B connector (USB) for connecting an external PC with installed Windows GUI control software.

Two input data signals supplied through the CML differential ports are sampled by an internal clock that is derived form an input half-rate clock.

The input clock has a controlled phase shift capability that allows for selection of the optimal data sampling point. The shifted clock is divided by 2, and supplied to two outputs through additional independent phase shifters. This feature is required for PAM4 signal generation using two MUX units. More details can be found in the AN_ASNT_MUX64 document.

A Windows GUI (compatible with Windows XP, 7, 8 and 10) is used to control all adjustable parameters of the unit including high speed data output amplitude, clock phase shifts, common-mode voltage levels of the input clock signals, etc.

The unit is powered by a single 9*V* supply delivered from an external AC-DC adapter connected to the input socket on the back panel.

An example of the output eye for a 56*Gbps* PRBS7 signal is shown in Fig. 3.

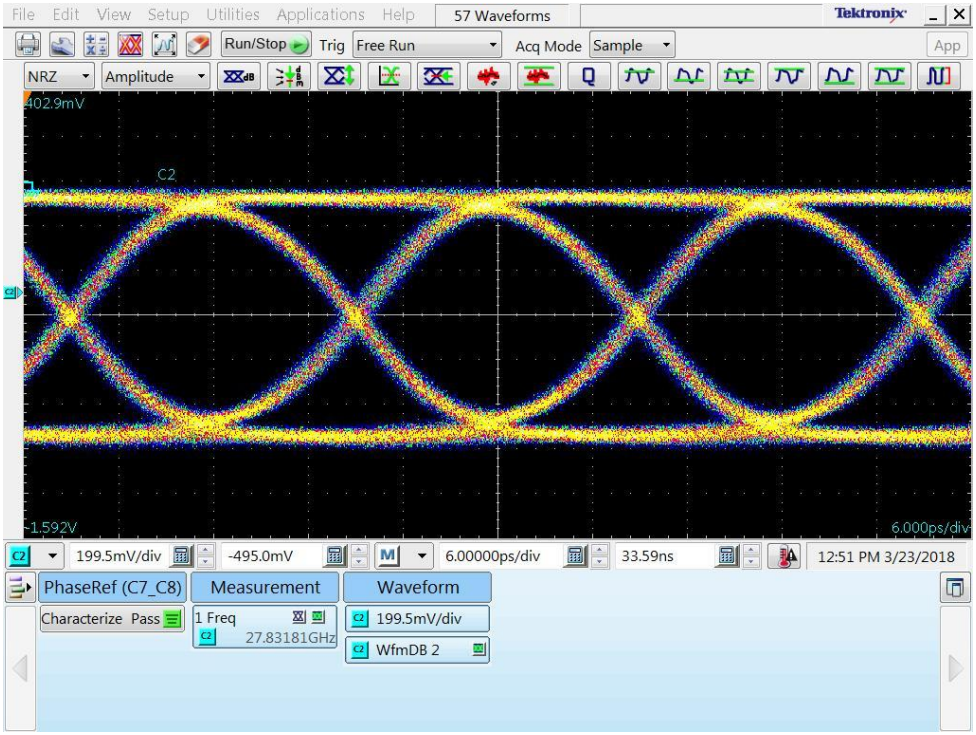

Fig. 3. Data Output Eye for 56Gbps PRBS7 signal

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All max voltage limits are referenced to ground.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)	6	12	*V*
Power Consumption		8	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
HS Input Clock					
Single-ended Swing	100		800	mV_{PP}	
Frequency	0.001		32	*GHz*	
HS Input Data					
Differential Swing	100		1000	mV_{PP}	Differential or Single-ended
Frequency	0.001		32	*Gbps*	
HS Output Clock					
Single-ended Swing		500		mV_{PP}	Typical
Frequency	0.0005		16	*GHz*	
HS Output Data					
Differential Swing		2000		mV_{PP}	
Common Mode Level		-0.5		*V*	
Data Rate	0.002		64	*Gbps*	
Rise/Fall times		7/7		*ps*	20% - 80%
Duty Cycle	40		60	*%*	Adjustable

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MECHANICAL DIMENSIONS

PARAMETER	TYP	UNIT	COMMENTS
Length	160	*mm*	
Width	103	*mm*	
Height	53	*mm*	

REVISION HISTORY

Revision	Date	Changes
2.1.2	07-2019	Updated Letterhead
2.1.1	05-2018	Updated Fig. 3
2.0.1	01-2018	Completely updated released
1.1.1	06-2015	Corrected Fig. 1
1.0.1	11-2014	Initial Release