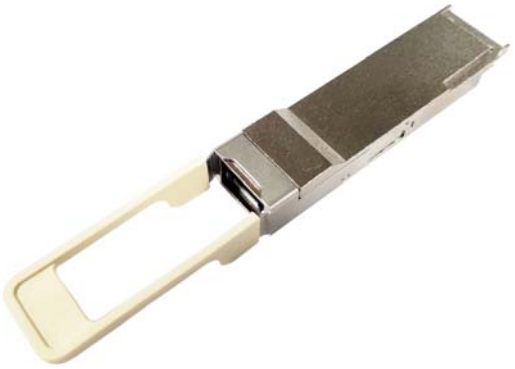
EOLQ-8540G-02-MO Series

Multi-Mode 40GBASE-SR4
QSFP+ Transceiver
RoHS Compliant



Features

- Compliant to the IEEE 802.3ba(40GBASE-SR4)
- Support interoperability with IEEE 802.3ae 10GBASE-SR modules of various form factors such as SFP+, XFP, X2
- Compliant to the QSFP+ MSA SFF-8436 Specification
- Up to 100m on OM3 and 150m on OM4 MMF
- VCSEL array transmitter and PIN array receiver
- Single 3.3V Power Supply and Power dissipation < 1.5W
- Operates at 10.3125Gbps per channel
- Operating Case Temperature: 0℃~+70℃
- I^2C interface with integrated Digital Diagnostic Monitoring
- Utilizes a standard 12/8 lane optical fiber with MPO connector
- Safety Certification: TUV/UL/FDA*Note1
- RoHS Compliant

Applications

- 40GBE and 10GBE interconnects
- Datacom/Telecom switch & router connections
- Data aggregation and backplane applications
- Proprietary protocol and density application

Ordering Information

Part No.	Data Rate	Fiber	Distance*(note2)	Interface	Temp.	DDMI
EOLQ-8540G-02-MO	40Gbps	MMF	100m/150m	MPO	0℃~+70℃	Yes

Note1: For the latest certification information, please check with Eoptolink.
Note2: 100m with OM3 MMF and 150m with OM4 MMF

*The product image only for reference purpose.

Absolute Maximum Ratings*

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%

*Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

Parameter	Symbol		Min.	Typical	Max.	Unit
Operating Case Temperature	T_C	EOLQ-8540G-02-MO	0		+70	°C
Power Supply Voltage	Vcc		3.135	3.3	3.465	V
Power Supply Current	Icc				450	mA
Aggregate Bit Rate	BR_{AVE}			41.25		Gbps
Lane Bit Rate	BR_{LANE}			10.3125		Gbps

Optical and Electrical Characteristics

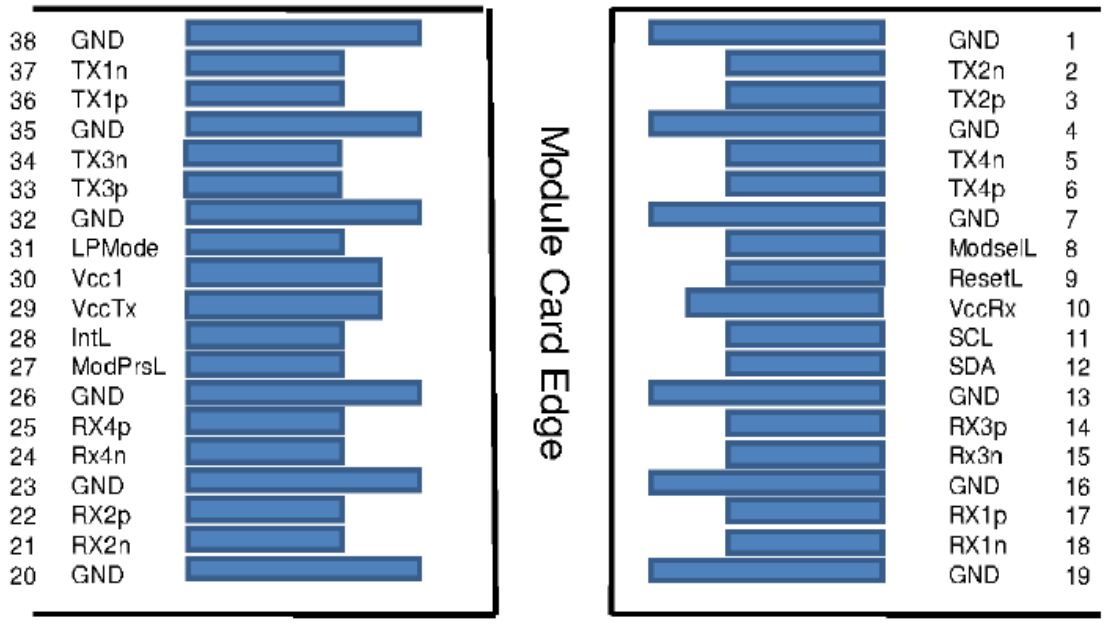
Parameter	Symbol	Min.	Typical	Max.	Unit
OM3 MMF	L	0.5	-	100	m
Aggregate Bit Rate	BR_{AVE}	-	40	-	Gbps
Per Lane Bit Rate	BR_{LANE}	-	10.3125	-	Gbps
Transmitter					
Center Wavelength	λ_C	840	850	860	nm
RMS spectral width	RMS	-	-	0.65	nm
Average Launch Power, Each Lane*(note3)	Pout/lane	-7.6	-	2.4	dBm
Transmit OMA, per Lane	TX_OMA/lane	-5.6	-	3	dBm
Difference in launch power between any two lanes(OMA)		-	-	4	dB
Peak power, each lane		-	-	4	dBm
Transmitter and dispersion penalty, each lane	TDP/lane	-	-	3.5	dB
Extinction Ratio*(note4)	ER	3	-	-	dB
Optical Return Loss Tolerance		-	-	12	dB
Average launch power of OFF, each lane		-	-	-30	dBm
Output Optical Eye*(note4)	IEEE 802.3ba-2010 Compliant				
Receiver					
Center Wavelength	λ_C	840	850	860	nm
Damage Threshold		3.4	-	-	dB
Stressed receiver sensitivity in OMA, each lane	Pmins	-	-	-5.4	dBm
Maximum Receive Power, each lane	Pmax	-	-	2.4	dBm
Average power, each lane	RX/lane	-9.5	-	+2.4	dBm

LOS De-Assert, OMA	LOSD	-	-	-7.5	dBm
Receiver reflectance	Rr	-	-	-12	dB
LOS Assert	LOSA	-30	-	-	dBm
LOS Hysteresis		0.5	-	-	dB

Note3: Output is coupled into a 50/125μm multi-mode fiber.

Note4: Filtered, measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps

QSFP+ Transceiver Electrical Pad Layout



Top Side
Viewed From Top

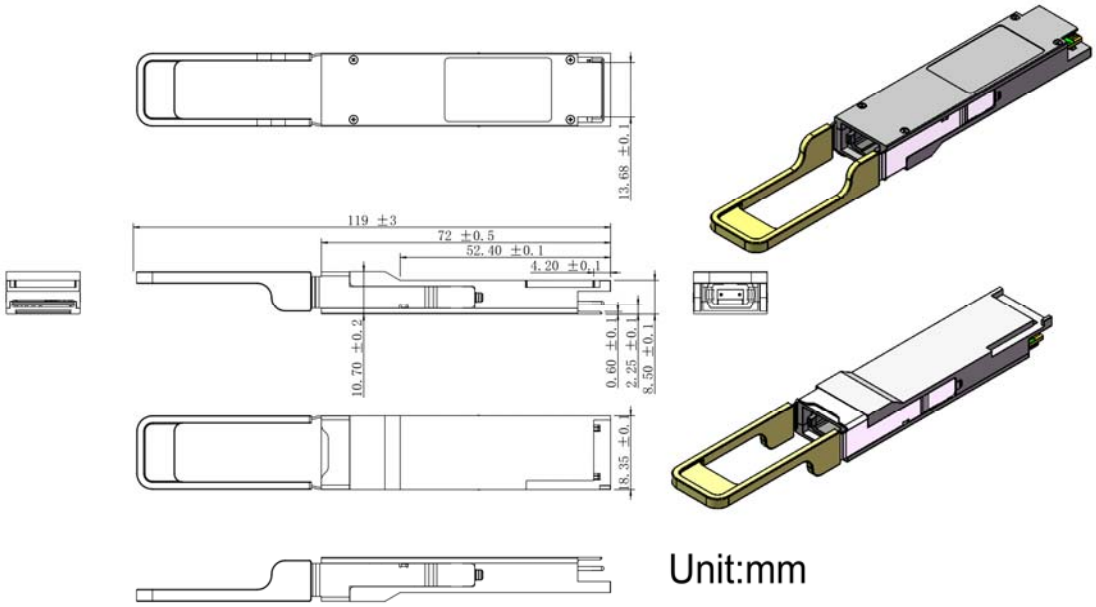
Bottom Side
Viewed From Bottom

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3	

13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1
1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.					
2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500mA.					

Mechanical Specifications



*This 2D drawing only for reference, please check with Eoptolink before ordering.

Obtaining Document

You can visit our website: http://www.eoptolink.com
Or contact Eoptolink Technology Inc., Ltd. listed at the end of the documentation to get the latest documents.

Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Kelly			Preliminary.	July 2, 2012
V1.b	Kelly			Correct digital interface.	Aug 7, 2012
V1.c	Kelly			Add photo.	Oct 30, 2012
V1.d	Abby	Kelly		Update min. RX/lane and Regulatory Compliance	Mar 20, 2014
V1.e	Abby	Kelly		Update max. RX/lane	April 18, 2014
V1.f	Abby	Kelly		Update Regulatory Compliance and Tr/Tf, Add J2, J9 Jitter	Dec 15, 2014
V1.g	Elaine/Peter	Torres/Kelly		Update 2D drawing & picture.	Feb 6, 2017
V1.h	Marvin	Kelly		Remove some describe about LOS ,2D drawing and regulatory compliance	Mar.9, 2017
V1.i	Marvin	Kelly		Update V1.h revision record: Modify the power	Apr 12, 2017

				dissipation and voltage tolerance. Remove input voltage tolerance, AC common tolerance, input impedance. Remove some describe about LOS, TX_DIS and FAULT. Remove output voltage tolerance, AC common tolerance, Termination, output impedance, remove rise/ fall Time. Modified 2D drawing and regulatory compliance	
V1.j	Marvin	Kelly/Chao. Wang/ Dean/Peter		Update the 2D drawing	Apr 28, 2017
V1.k	Nico	Kelly/Marvin /Peter		Update the product image, regulatory compliance, 2D drawing and contact	Aug 15, 2018
V1.l	Angela	Kelly/ Yiwei.Chen		Updated the regulatory compliance information.	December 14, 2018

Notice:

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