EOLS-BI1603-29X 34X 36X Series

Single-Mode 155Mbps SDH /SONET
Simplex LC or SC Single-Fiber SFP Transceiver
RoHS6 Compliant

Features

- Support 155Mbps data links
- 18-Wavelength CWDM DFB LD Transmitter from 1270nm to 1610nm, with step 20nm
- Single 3.3V Power supply and TTL Logic Interface
- Hot-Pluggable SFP Footprint Simplex LC Connector Interface
- Class 1 FDA and IEC60825-1 laser safety compliant
- Operating Case Temperature
  Standard: 0℃~+70℃
  Extended: -20℃~+85℃
- Compliant with SFP MSA
- Compliant with SFF-8472

Applications

- SONET OC-3 / SDH STM-1
- WDM Fast Ethernet Links

Ordering information

Part No.	Data Rate	Power budget	Interface	Temp.	DDMI
EOLS-BI1603-29XX*(note1)	100M~155Mbps	≥29dB	SC	Standard	NO
EOLS-BI1603-29XXI	100M~155Mbps	≥29dB	SC	Extended	NO
EOLS-BI1603-29XXD	100M~155Mbps	≥29dB	SC	Standard	YES
EOLS-BI1603-29XXDI	100M~155Mbps	≥29dB	SC	Extended	YES
EOLS-BI1603-29XXL*(note1)	100M~155Mbps	≥29dB	LC	Standard	NO
EOLS-BI1603-29XXIL	100M~155Mbps	≥29dB	LC	Extended	NO
EOLS-BI1603-29XXDL	100M~155Mbps	≥29dB	LC	Standard	YES
EOLS-BI1603-29XXDIL	100M~155Mbps	≥29dB	LC	Extended	YES
EOLS-BI1603-34XX*(note1)	100M~155Mbps	≥34dB	SC	Standard	NO
EOLS-BI1603-34XXI	100M~155Mbps	≥34dB	SC	Extended	NO

EOLS-BI1603-34XXD	100M~155Mbps	⩾34dB	SC	Standard	YES
EOLS-BI1603-34XXDI	100M~155Mbps	⩾34dB	SC	Extended	YES
EOLS-BI1603-34XXL*(note1)	100M~155Mbps	⩾34dB	LC	Standard	NO
EOLS-BI1603-34XXIL	100M~155Mbps	⩾34dB	LC	Extended	NO
EOLS-BI1603-34XXDL	100M~155Mbps	⩾34dB	LC	Standard	YES
EOLS-BI1603-34XXDIL	100M~155Mbps	⩾34dB	LC	Extended	YES
EOLS-BI1603-36XX*(note1)	100M~155Mbps	⩾36dB	SC	Standard	NO
EOLS-BI1603-36XXI	100M~155Mbps	⩾36dB	SC	Extended	NO
EOLS-BI1603-36XXD	100M~155Mbps	⩾36dB	SC	Standard	YES
EOLS-BI1603-36XXDI	100M~155Mbps	⩾36dB	SC	Extended	YES
EOLS-BI1603-36XXL*(note1)	100M~155Mbps	⩾36dB	LC	Standard	NO
EOLS-BI1603-36XXIL	100M~155Mbps	⩾36dB	LC	Extended	NO
EOLS-BI1603-36XXDL	100M~155Mbps	⩾36dB	LC	Standard	YES
EOLS-BI1603-36XXDIL	100M~155Mbps	⩾36dB	LC	Extended	YES

Note1: Standard version, X refer to CWDM Wavelength range 1270nm to 1610nm, A=1270, B=1290…Q=1590, R=1610. TX and RX wavelength spacing must ⩾60nm. Typical transmitter and receiver wavelength combinations are L/O, M/Q, M/P and etc.

*The product image only for reference purpose.

CWDM* Wavelength

Band	Nomenclature	Wavelength(nm)		
		Min.	Typ.	Max.
O-band Original	A	1264	1270	1277.5
	B	1294	1290	1297.5
	C	1304	1310	1317.5
	D	1324	1330	1337.5
	E	1344	1350	1357.5
E-band Extended	F	1364	1370	1377.5
	G	1384	1390	1397.5
	H	1404	1410	1417.5
	I	1424	1430	1437.5
	J	1444	1450	1457.5
S-band Short Wavelength	K	1464	1470	1477.5
	L	1484	1490	1497.5
	M	1504	1510	1517.5
	N	1524	1530	1537.5
C-band Conventional	O	1544	1550	1557.5
L-band Long Wavelength	P	1564	1570	1577.5
	Q	1584	1590	1597.5
	R	1604	1610	1617.5

CWDM*: 18 Wavelengths from 1270nm to 1610nm, each step 20nm.

Regulatory Compliance*

Product Certificate	Certificate Number	Applicable Standard
TUV	R50135086	EN 60950-1:2006+A11+A1+A12+A2
		EN 60825-1:2014
		EN 60825-2:2004+A1+A2
UL	E317337	UL 60950-1
		CSA C22.2 No. 60950-1-07
EMC CE	AE 50384190 0001	EN 55032:2012
		EN 55032:2015
		EN 55024:2010
		EN 55024:2010+A1
FCC	WTF14F0514417E	47 CFR PART 15 OCT., 2013
FDA	/	CDRH 1040.10
ROHS	/	2011/65/EU

*The above certificate number updated to June 2018, because some certificate will be updated every year, such as FDA and ROHS. For the latest certification information, please check with Eoptolink.

Product Description

The EOLS-BI1603-XX series is small form factor pluggable module for IEEE 802.3ah 1000BASE-BX and OC-3/STM-1 SONET/SDH single fiber communications. It is with the SFP 20-pin connector to allow hot plug capability.

The EOLS-BI1603-XX series are designed to be compliant with SFF-8472.

Absolute Maximum Ratings*note2

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V
Operating Relative Humidity		-	95	%

Note2: Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

Parameter		Symbol		Min.	Typical	Max.	Unit
Operating Case Temperature		Tc	EOLS-BI1603-XX	0		+70	°C
			EOLS-BI1603-XXI	-20		+85	
Power Supply Voltage		V_{CC}		3.15	3.3	3.45	V
Power Supply Current		I_{CC}				300	mA
Date Rate	OC-3				155		Mbps
	100M				100		Mbps

Performance Specifications – Electrical

Parameter		Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter							
LVPECL Inputs(Differential)		Vin	400		2000	mVpp	AC coupled inputs*(note5)
Input Impedance (Differential)		Zin	85	100	115	ohms	Rin > 100 kohms @ DC
Tx_Dis	Disable		2		Vcc	V	
	Enable		0		0.8		
Tx_FAULT	Fault		2		Vcc+0.3	V	
	normal		0		0.5		
Receiver							
LVPECL Outputs (Differential)		Vout	370		2000	mVpp	AC coupled outputs*(note5)
Output Impedance (Differential)		Zout	85	100	115	ohms	
Rx_LOS	LOS		2		Vcc+0.3	V	
	normal		0		0.8	V	
MOD_DEF (0:2)		VoH	2.5			V	With Serial ID
		VoL	0		0.5	V	

Performance Specifications – Optical

(CWDM DFB and PIN-TIA with 29dB Power Budget)

Parameter		Symbol	Min.	Typical	Max.	Unit
Power budget			29			dB
Data Rate				100/155		Mbps
Transmitter						
Channel Centre Wavelength*(note9)			λ_C-6	λ_C	λ_C+7.5	nm
Spectral Width (-20dB)		Δλ			1	nm
Side Mode Suppression Ratio		SMSR	30			dB
Average Output Power*(note3)		Pout	-5		0	dBm
Extinction Ratio*(note4)		ER	10			dB
Rise/Fall Time(20%～80%)		tr/tf			2	ns
Output Optical Eye*(note4)		IUT-T G.957 Compliant*(note7)				
TX_Disable Assert Time		t_off			10	Us
Receiver						
Channel Centre Wavelength*(note9)			1260		1630	nm
Receiver Sensitivity*(note6)	OC-3	Pmin			-34	dBm
	100M				-35	dBm
Receiver Overload		Pmax	-10			dBm
Return Loss			12			dB

Optical Path Penalty				1	dB
LOS De-Assert	LOSD			-36	dBm
LOS Assert	LOSA	-45			dBm
LOS Hysteresis*(note8)		0.5			dB

(CWDM DFB and PIN-TIA with 34dB Power Budget)

Parameter	Symbol	Min.	Typical	Max.	Unit
Power budget		34			dB
Data Rate			100/155		Mbps
Transmitter					
Channel Centre Wavelength*(note9)		λc-6	λc	λc+7.5	nm
Spectral Width (-20dB)	Δλ			1	nm
Side Mode Suppression Ratio	SMSR	30			dB
Average Output Power*(note3)	Pout	0		5	dBm
Extinction Ratio*(note4)	ER	10			dB
Rise/Fall Time(20%～80%)	tr/tf			2	ns
Output Optical Eye*(note4)	IUT-T G.957 Compliant*(note7)				
TX_Disable Assert Time	t_off			10	Us
Receiver					
Channel Centre Wavelength*(note9)		1260		1630	nm
Receiver Sensitivity @ EOL*(note6) OC-3	Pmin, EOL			-34	dBm
Receiver Sensitivity @ EOL*(note6) 100M	Pmin, EOL			-35	dBm
Receiver Overload	Pmax	-10			dBm
Return Loss		12			dB
Optical Path Penalty				1	dB
LOS De-Assert	LOSD			-36	dBm
LOS Assert	LOSA	-45			dBm
LOS Hysteresis*(note8)		0.5			dB

(CWDM DFB and PIN-TIA with 36dB Power Budget)

Parameter	Symbol	Min.	Typical	Max.	Unit
Power budget		36			dB
Data Rate			100/155		Mbps
Transmitter					
Channel Centre Wavelength*(note9)		λc-6	λc	λc+7.5	nm
Spectral Width (-20dB)	Δλ			1	nm
Side Mode Suppression Ratio	SMSR	30			dB
Average Output Power*(note3)	Pout	+1		+5	dBm
Extinction Ratio*(note4)	ER	10			dB
Rise/Fall Time(20%～80%)	tr/tf			2	ns
Output Optical Eye*(note4)	IUT-T G.957 Compliant*(note7)				
TX_Disable Assert Time	t_off			10	Us
Receiver					
Channel Centre Wavelength*(note9)		1260		1630	nm

Receiver Sensitivity @ EOL*(note6)	OC-3	Pmin,			-35	dBm
	100M				-36	dBm
Receiver Overload		Pmax	-10			dBm
Return Loss			12			dB
Optical Path Penalty					1	dB
LOS De-Assert		LOSD			-37	dBm
LOS Assert		LOSA	-45			dBm
LOS Hysteresis*(note8)			0.5			dB

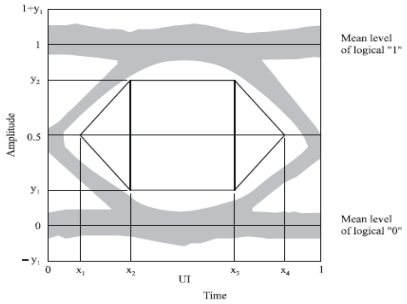
Note3: Output is coupled into a 9/125μm single-mode fiber.

Note4: Filtered, measured with a PRBS 2^{23}-1 test pattern @155Mbps

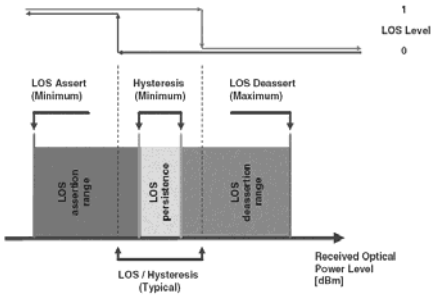
Note5: LVPECL logic, internally AC coupled.

Note6: Minimum average optical power measured at the BER less than 1E-10 with a 2^{23}-1 PRBS and ER=9 dB.

Note7: Eye pattern mask

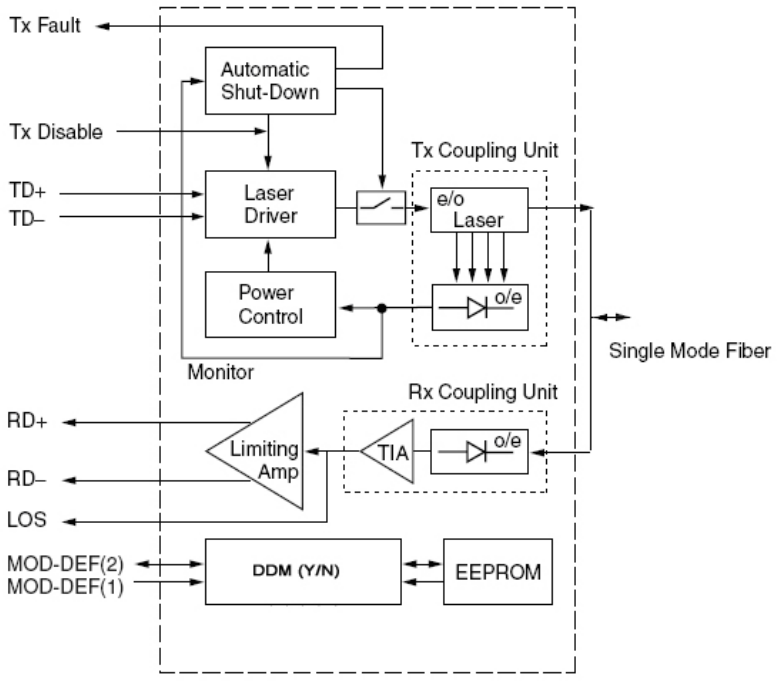


Note8: LOS Hysteresis

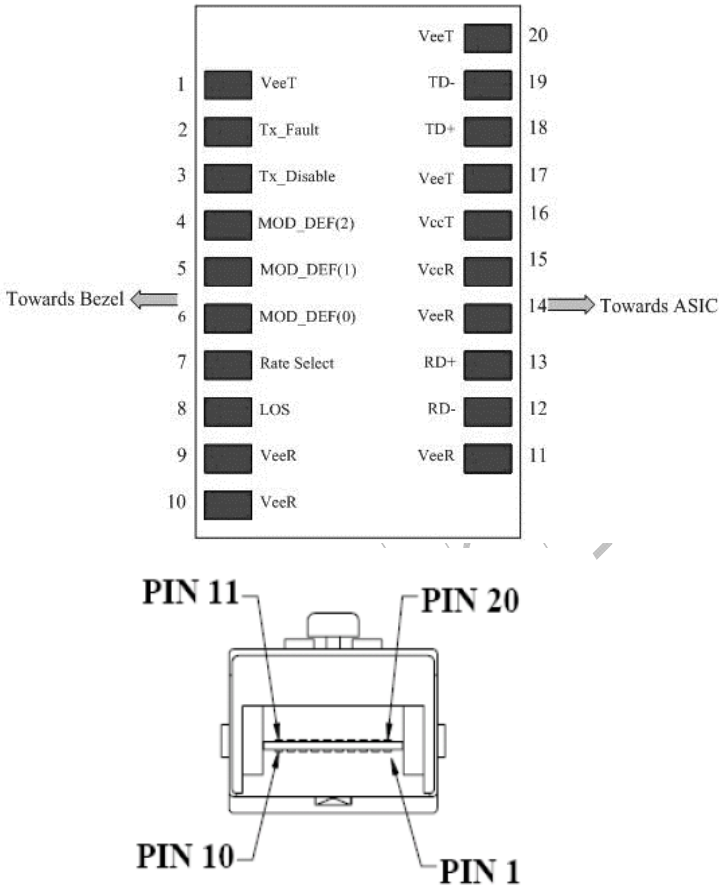


Note9: The channel center wavelength of transmitter side is compliant with table <CWDM* Wavelength>, and the channel center wavelength of receiver side is the typical wavelength of CWDM channel ±20nm.

Functional Description of Transceiver



SFP Transceiver Electrical Pad Layout



Pin Function Definitions

Pin Num.	Name	FUNCTION	Plug Seq.	Notes
1	VeeT	Transmitter Ground	1	5)
2	TX Fault	Transmitter Fault Indication	3	1)
3	TX Disable	Transmitter Disable	3	2), Module disables on high or open
4	MOD-DEF2	Module Definition 2	3	3), Data line for Serial ID.
5	MOD-DEF1	Module Definition 1	3	3), Clock line for Serial ID.
6	MOD-DEF0	Module Definition 0	3	3), Grounded within the module.
7	Rate Select	Not Connect	3	Function not available
8	LOS	Loss of Signal	3	4)
9	VeeR	Receiver Ground	1	5)
10	VeeR	Receiver Ground	1	5)
11	VeeR	Receiver Ground	1	5)
12	RD-	Inv. Received Data Out	3	6)

13	RD+	Received Data Out	3	7)
14	VeeR	Receiver Ground	1	5)
15	VccR	Receiver Power	2	3.3 ± 5%, 7)
16	VccT	Transmitter Power	2	3.3 ± 5%, 7)
17	VeeT	Transmitter Ground	1	5)
18	TD+	Transmit Data In	3	8)
19	TD-	Inv. Transmit Data In	3	8)
20	VeeT	Transmitter Ground	1	5)

Notes:

1) TX Fault is an open collector/drain output, which should be pulled up with a 4.7K – 10KΩ resistor on the host board. Pull up voltage between 2.0V and VccT, R+0.3V. When high, output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.

2) TX disable is an input that is used to shut down the transmitter optical output. It is pulled up within the module with a 4.7 – 10 K Ω resistor. Its states are:
Low (0 – 0.8V): Transmitter on
(>0.8, < 2.0V): Undefined
High (2.0 – 3.465V): Transmitter Disabled
Open: Transmitter Disabled

3) Mod-Def 0,1,2. These are the module definition pins. They should be pulled up with a 4.7K – 10Kωresistor on the host board. The pull-up voltage shall be VccT or VccR (see Section IV for further details). Mod-Def 0 is grounded by the module to indicate that the module is present Mod-Def 1 is the clock line of two wire serial interface for serial ID Mod-Def 2 is the data line of two wire serial interface for serial ID

4) LOS (Loss of Signal) is an open collector/drain output, which should be pulled up with a 4.7K – 10KΩ resistor. Pull up voltage between 2.0V and VccT, R+0.3V. When high, this output indicates the received optical power is below the worst-case receiver sensitivity (as defined by the standard in use). Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.

5) VeeR and VeeT may be internally connected within the SFP module.

6) RD-/+: These are the differential receiver outputs. They are AC coupled 100Ω differential lines which should be terminated with 100Ω (differential) at the user SERDES. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 370 and 2000 mV differential (185 –1000 mV single ended) when properly terminated.

7) VccR and VccT are the receiver and transmitter power supplies. They are defined as 3.3V ±5% at the SFP connector pin. Maximum supply current is 300mA. Recommended host board power supply filtering is shown below. Inductors with DC resistance of less than 1 ohm should be used in order to maintain the required voltage at the SFP input pin with 3.3V supply voltage. When the recommended supply-filtering network is used, hot plugging of the SFP transceiver module will result in an inrush current of no more than 30mA greater than the steady state value. VccR and

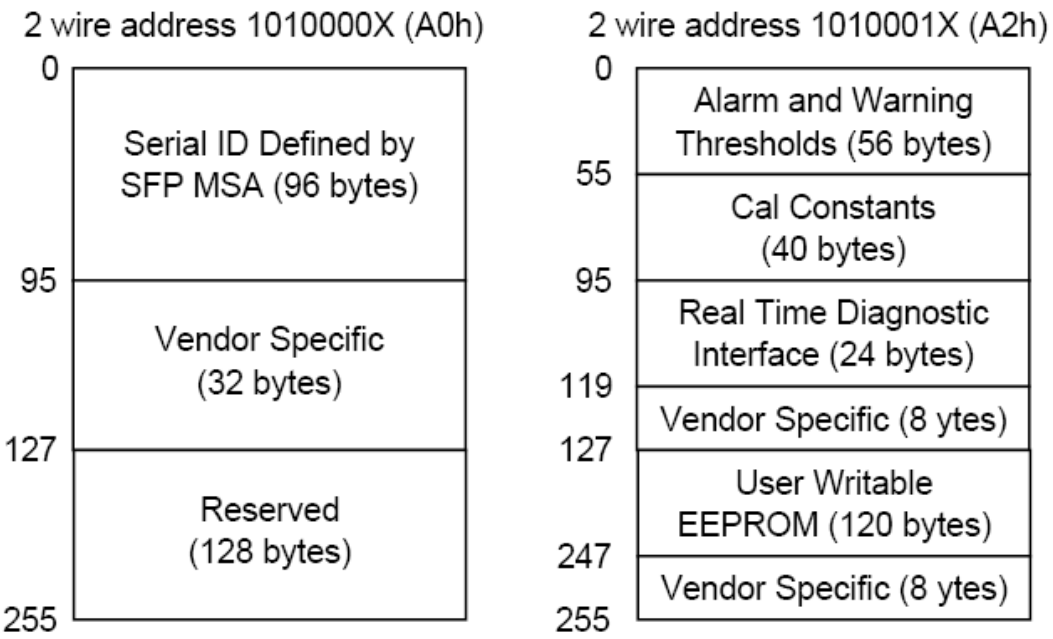
VccT may be internally connected within the SFP transceiver module.

8) TD-/+: These are the differential transmitter inputs. They are AC-coupled, differential lines with 100Ω differential termination inside the module. The AC coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 500 – 2400 mV (250 – 1200mV single-ended), though it is recommended that values between 500 and 1200 mV differential (250 – 600mV single-ended) be used for best EMI performance.

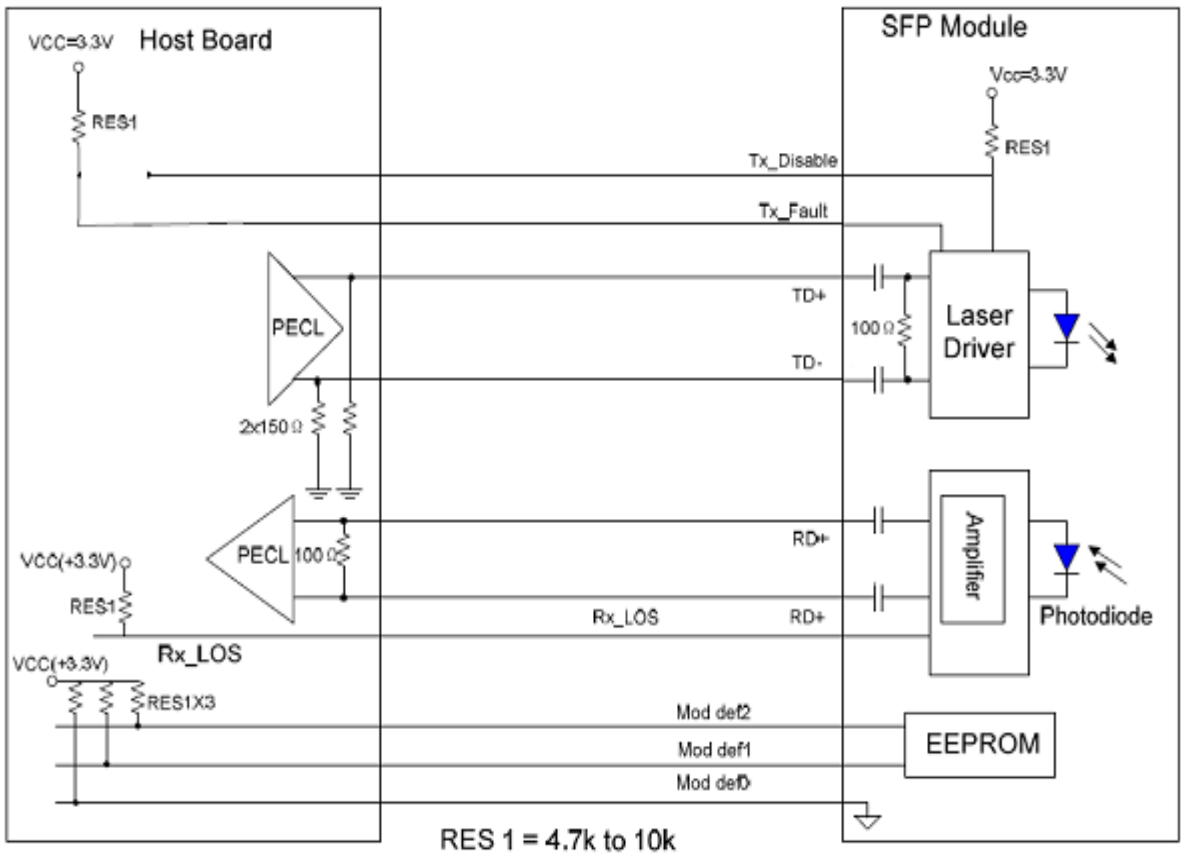
EEPROM

The serial interface uses the 2-wire serial CMOS EEPROM protocol defined for the ATMEL AT24C02/04 family of components. When the serial protocol is activated, the host generates the serial clock signal (SCL). The positive edge clocks data into those segments of the EEPROM that are not write protected within the SFP transceiver. The negative edge clocks data from the SFP transceiver. The serial data signal (SDA) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

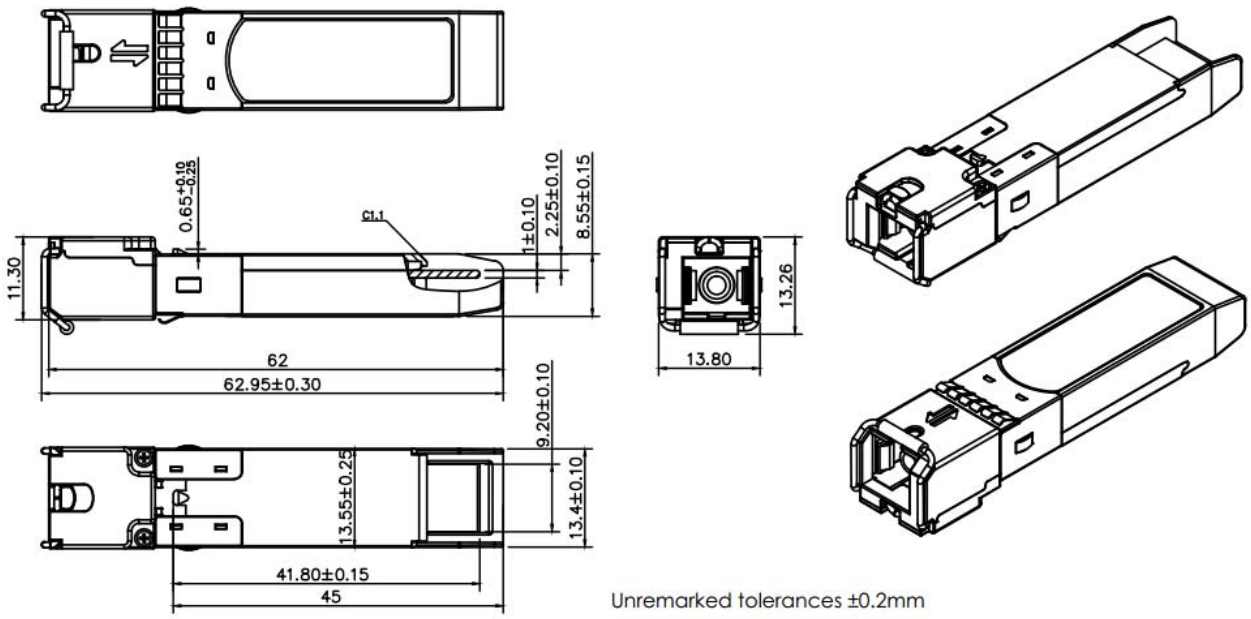
The Module provides diagnostic information about the present operating conditions. The transceiver generates this diagnostic data by digitization of internal analog signals. Calibration and alarm/warning threshold data is written during device manufacture. Received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring all are implemented. The diagnostic data are raw A/D values and must be converted to real world units using calibration constants stored in EEPROM locations 56 – 95 at wire serial bus address A2h. The digital diagnostic memory map specific data field define as following .For detail EEPROM information, please refer to the related document of SFF 8472 Rev 9.3.



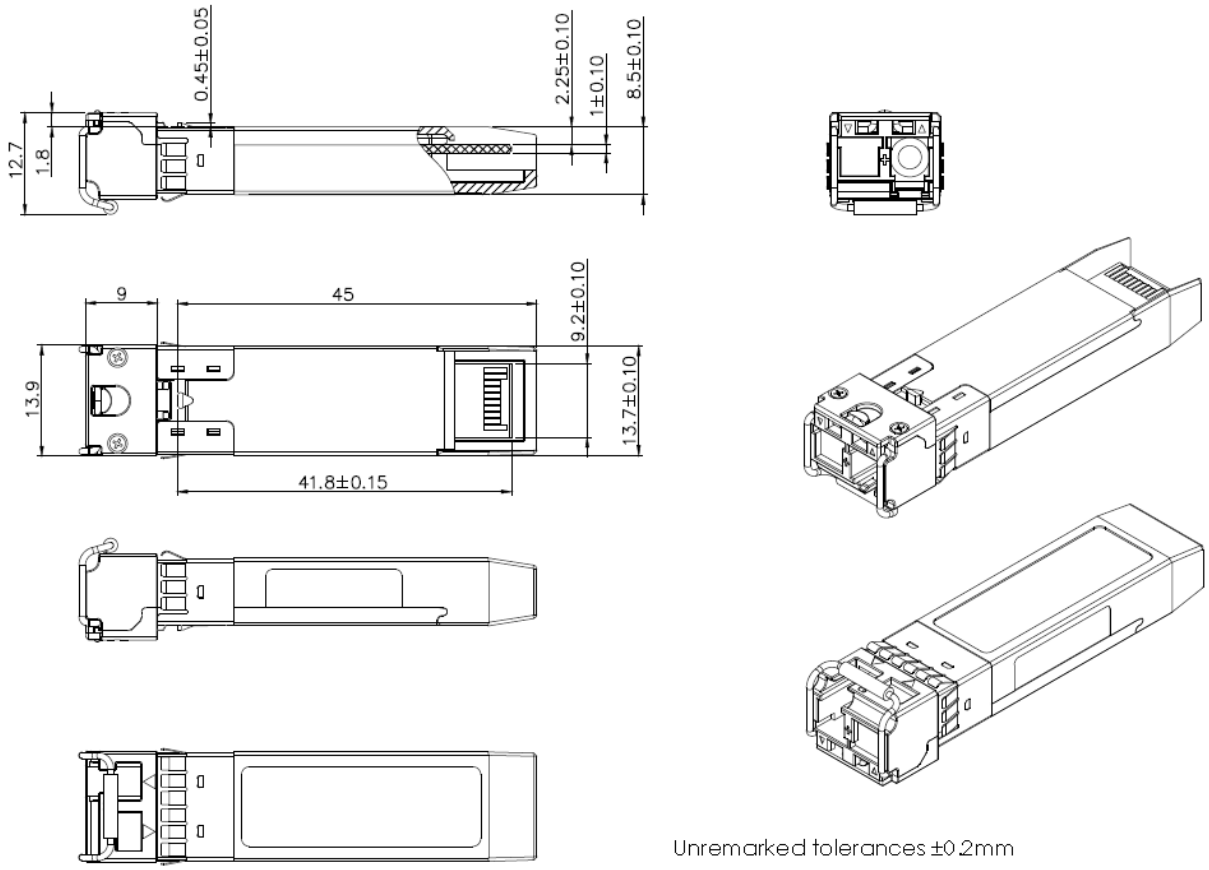
Recommend Circuit Schematic



Mechanical Specifications



SC



LC

*This 2D drawing only for reference, please check with Eoptolink before ordering.

Laser Emission

Obtaining Document

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Revision History

Revision	Initiate	Review	Approve	Revision History	Data
V1.a	Cathy	Kelly		Released.	2009.09.10
V1.b	Cathy	Kelly		Update the mechanical specl	2010.1.23
V1.c	Cathy			Updated EEPROM.	2011.3.11
V2.a	Phlio			Update Recommend Circuit	Aug 10, 2011
V3.a	Phlio			Remove EEPROM Detail Information Change Power Link Budget	Aug 22, 2011
V3.b	Kelly			Update photo.	Nov 4, 2011
V3.c	Philo/Angela	Kelly		Update temp. range and LOSD&LOSA	Nov 27,2012
V3.d	Abby/ Walt	Kelly/Jason/Lyn/ Walt/Arvin/Nygai		Update Extended Temperature, Regulatory Compliance and Extinction Ratio.	Oct 26, 2013
V3.e	Angela	Kelly/Vina/Dean /Chao.Wang		Update the regulatory compliance and 2D drawing.	July 21, 2017
V3.f	Angela	Yiwei.Chen		Update the regulatory compliance.	August 7, 2018

Notice:

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