RDA012LP

12 Bit 1.5 GS/s Low Power DAC

Features

- 12 Bit Resolution
- 1.5 GS/s Sampling Rate
  2.0 GS/s typical
- Differential Analog Output
- Output Signal: 0dBm
- Offset Binary Input Code Format
- DNL: ±2 LSB
- INL: ±2 LSB
- SFDR: 63dBc at Fclk=1GHz with Fout=340MHz
- SFDR: 59dBc at Fclk=1.5GHz with Fout=510MHz
- SFDR: 53dBc at Fclk=2GHz with Fout=680MHz
- 3.3V Power Supply
- 700mW Power Dissipation
- 32 Lead QFP package

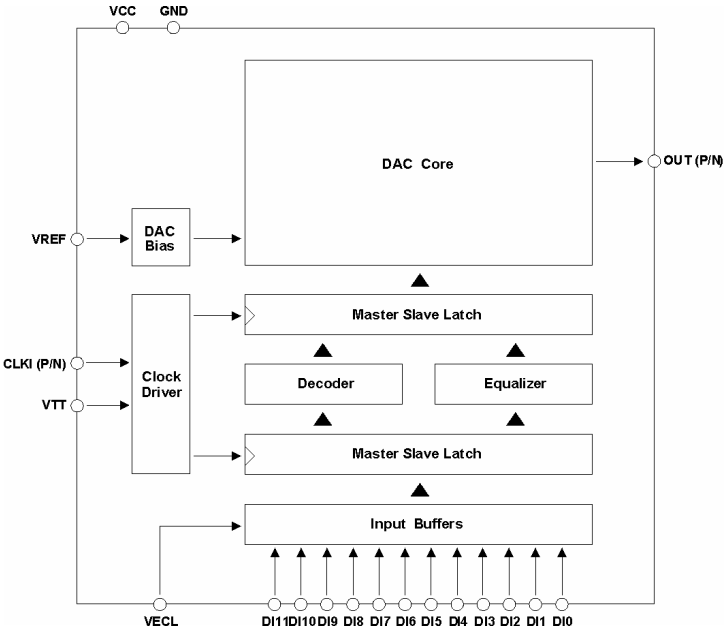

Figure 1 - Functional Block Diagram

Product Description

The RDA012LP is a low-power 12 bit digital to analog converter (DAC) with a data sampling rate of 1.5GS/s (works with clock frequencies above 2.0GHz). The RDA012LP has been optimized for applications demanding for a high performance low-power DAC, achieving 63 dBc of spurious free dynamic range (SFDR) at 1 GS/s and f_{out} of 333 MHz. The DAC utilizes a segmented current source to reduce glitch energy and achieve high linearity performance. For better dynamic performance, the DAC outputs are internally terminated with 50Ω resistance. It outputs a nominally 0dBm of power when terminated with external 50Ω resistors.

Ordering information

PART NUMBER	DESCRIPTION
RDA012LP-QP	12 BIT 1.5GS/s DAC, QFP Package
RDA012LP-DI	12 BIT 1.5GS/s DAC, DIE
EVRDA012LP-QP	RDA012LP-QP Evaluation Board

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

Between GNDs ……..……-0.3 to +0.3 V
Between VCCs ……..…….. -0.3 to +0.3 V
VCCs to GND ……..…… 0 V to +3.8 V

RF Input Voltages

CLKIP, CLKIN to GND .....…… 0 V to VCC

HS Digital Input Voltages

DI<0:11> ..... 0 V to VCC

Output Termination Voltages

DOUTP, DOUTN to GND ……..……. 0 V to VCC

Temperature

Case Temperature…… -15 to +85 °C
Junction Temperature……..…….. +120 °C
Lead, Soldering (10 Seconds) ……..…….. +220 °C
Storage…..…….. -40 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 3.3V; VREF = 1.3V; VECL = 2V; VTT = 1.3V; Clock: 1.5GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to VCC.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Differential Nonlinearity	DNL	Maximum of Absolute Value		2		LSB
1.2	Integral Nonlinearity	INL	Maximum of Absolute Value		2		LSB
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up			30	s
3.0	**CLOCK INPUT (CLKIP, CLKIN)**						
3.1	Input Resistance	R_{CLKI}	Resistance (CLKI P/N) to VTT		50		Ω
4.0	**DIGITAL INPUTS (DI<0:11>)**						
4.1	Input Resistance	R_{DIN}			50		Ω
5.0	**ANALOG OUTPUTS (OUTP, OUTN)**						
5.1	Full-scale Output Swing	V_{FSD}	Differential, Terminated Into 50Ω to VCC=3.3V on Each Output		600		mVpp
5.2	Full-scale Output Swing	V_{FSS}	Single Ended, Terminated Into 50Ω to VCC=3.3V		300		mVpp
5.3	Full-scale Output Range	V_{FSRS}	Single Ended, Terminated Into 50Ω to VCC=3.3V (MIN=000h, MAX=FFFh)	3.0		3.3	V
6.0	**POWER SUPPLY REQUIREMENTS**						
6.1	Positive Current	ICC			210		mA
6.2	Power Dissipation	P			700		mW

AC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VCC = 3.3V; VREF = 1.3V; VECL = 2V; VTT = 1.3V; Clock: 1.5GHz, 0.6Vpp Differential; Outputs Terminated Into 50 Ω to VCC.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
7.0	**DYNAMIC PERFORMANCE**						
7.1	Spurious Free Dynamic Range	SFDR1	F_{clk} = 1000MHz , F_{out} = 63MHz		66		dBc
7.2		SFDR2	F_{clk} = 1000MHz , F_{out} = 340MHz		63		dBc
7.3		SFDR3	F_{clk} = 1200MHz , F_{out} = 76MHz		64		dBc
7.4		SFDR4	F_{clk} = 1200MHz , F_{out} = 408MHz		61		dBc
7.5		SFDR5	F_{clk} = 1300MHz , F_{out} = 82MHz		63		dBc
7.6		SFDR6	F_{clk} = 1300MHz , F_{out} = 445MHz		60		dBc
7.7		SFDR7	F_{clk} = 1500MHz , F_{out} = 95MHz		61		dBc
7.8		SFDR8	F_{clk} = 1500MHz , F_{out} = 390MHz		59		dBc
7.9		SFDR9	F_{clk} = 1500MHz , F_{out} = 510MHz		59		dBc
7.10		SFDR10	F_{clk} = 2000MHz , F_{out} = 125MHz		60		dBc
7.11		SFDR11	F_{clk} = 2000MHz , F_{out} = 680MHz		53		dBc
8.0	**ANALOG OUTPUTS (OUTP, OUTN)**						
8.1	Rise Time	$T_{R,OUT}$			350		ps
8.2	Fall Time	$T_{F,OUT}$			350		ps

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
9.0	**CLOCK INPUTS (CLKIP, CLKIN)**						
9.1	Amplitude	$V_{CPP,HCLKI}$		200		1000	mV
9.2	Common Mode Voltage	$V_{CCM,HCLKI}$					V
9.3	Maximum Frequency	$F_{MAX,HCLKI}$		1500	2000		MHz
10.0	**DIGITAL INPUTS (DI<0:11>)**						
10.1	Input High Voltage	$V_{IH,DIN}$	V_{ECL} = 2V	2.1		3	V
10.2	Input Low Voltage	$V_{IL,DIN}$	V_{ECL} = 2V	0		1.9	V
11.0	**TERMINATION VOLTAGE (VTT)**						
11.1	Reference Voltage	V_{TT}	Termination Voltage for CLKI		1.3		V
12.0	**REFERENCE (VECL)**						
12.1	Reference Voltage	V_{ECL}	Reference Voltage for DI<0:11>	1.2	2		V
13.0	**REFERENCE (VREF)**						
13.1	Reference Voltage	V_{REF}			1.3		V
14.0	**POWER SUPPLY REQUIREMENTS**						
14.1	Positive Supply Voltage	VCC		3.1	3.3	3.5	V
15.0	**OPERATING TEMPERATURE**						
15.1	Case Temperature	Tc	Measured at Bottom Plate	-15		85	°C
15.2	Junction Temperature	Tj				120	°C

Pin Description and Pin Layout

P/I/O	PIN	NUM.	NAME	FUNCTION
P	10, 16, 17, 18, 23, 24, 25, bottom plate	8	VCC	Power Supply
P	13, 19, 20, 21, 22, 27	6	GND	Ground
I	31	1	VECL	2V Reference Voltage for Input
I	26	1	VREF	1.3V External Reference Voltage
I	29	1	VTT	1.3V Clock Termination Voltage
I	28	1	CLKIP	Clock Input
I	30	1	CLKIN	
I	12, 11, 9, 8, 7, 6, 5, 4, 3, 2, 1, 32	12	DI<0-11>	DI<i> Is Digital Bit i Input. MSB is bit 11.
O	15	1	OUTP	Differential Output
O	14	1	OUTN	

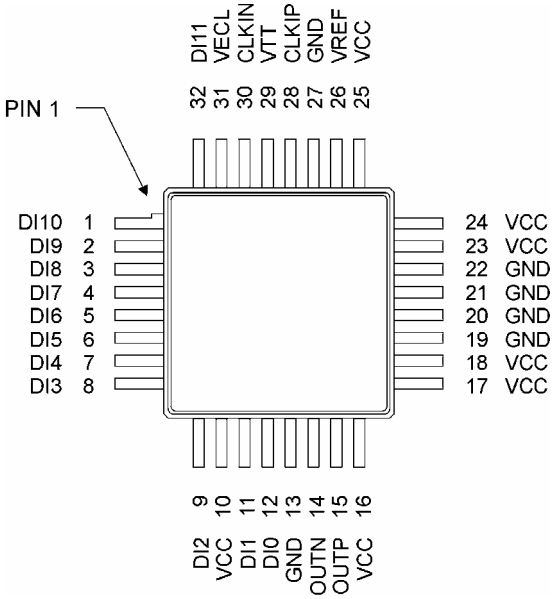

Figure 2 - RDA012LP-QP pinout (top view).

Die Pad Layout

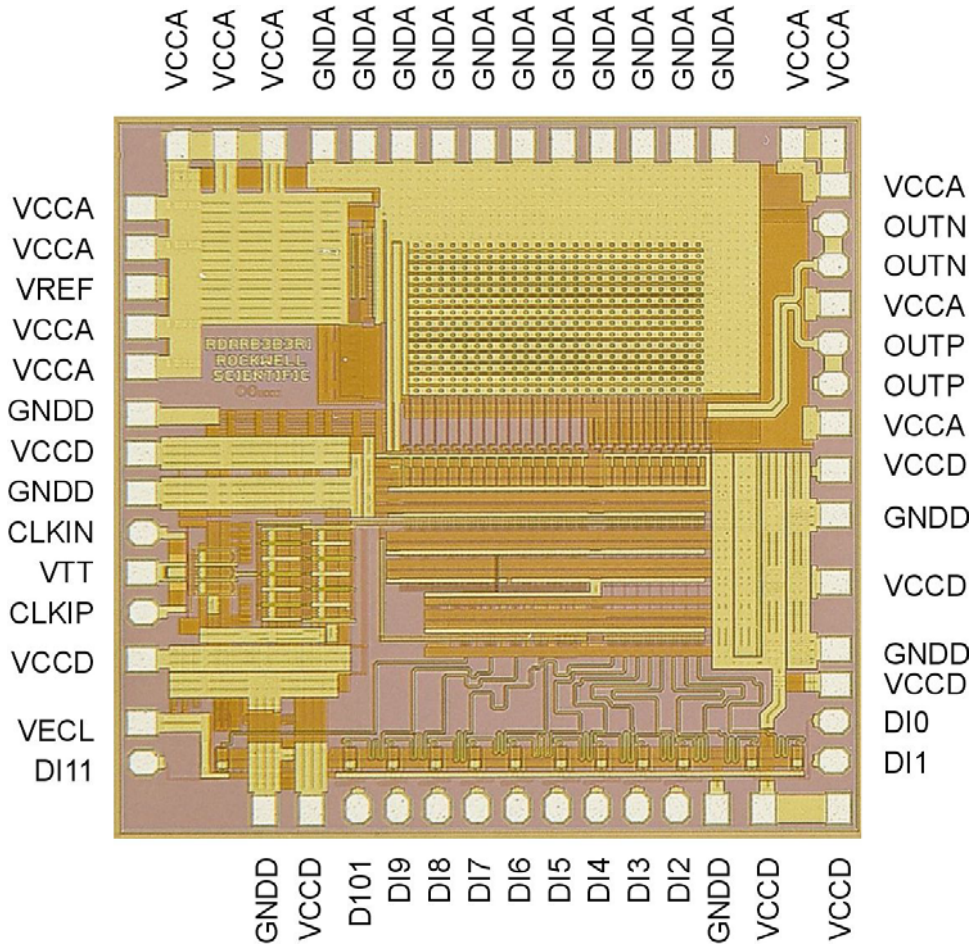

Figure 3 – RDA012LP die pad layout.

Theory of Operation

For best dynamic and static performance, the RDA012LP DAC employs 4 Bit segmentation. The LVPECL compatible 12 Bit digital data inputs are latched by master-slave flip-flops immediately after the input buffer to reduce the data skew. The 4 MSB data bits are decoded into thermometer code by a two-stage decoding block, and the 8 LSB data bits are transported through the delay equalizer block. The digital data are then synchronized again by a second master-slave flip-flop to reduce the switching glitch. The decoded 4 MSB data drive 15 identical current switches, and the 8 LSB data drive 8 current switches. The output nodes from the LSB current switches are connected to the analog output through an R-2R ladder to generate the binary output. The RDA012LP DAC provides output terminated at 50Ω, illustrated in an equivalent circuit in Figure 5. The output full-scale voltage follows the relationship V_{FS} = 0.3xV_{REF}. The VREF pin supplies the reference voltage for the DAC core and is recommended that an accurate, temperature-compensated voltage reference be used.

Equivalent Circuit

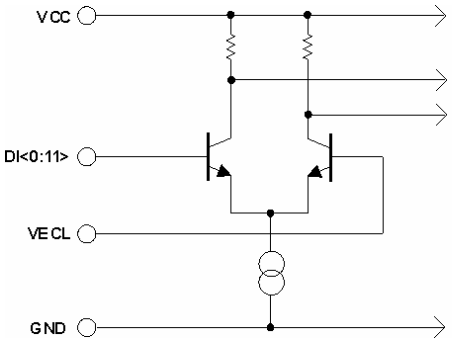

Figure 4 – Data input circuit.

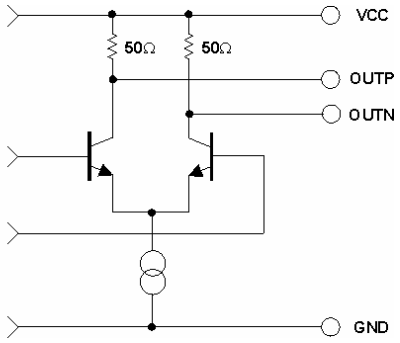

Figure 5 – Output circuit.

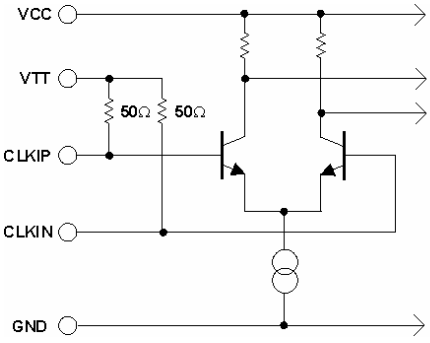

Figure 6 – Clock input circuit.

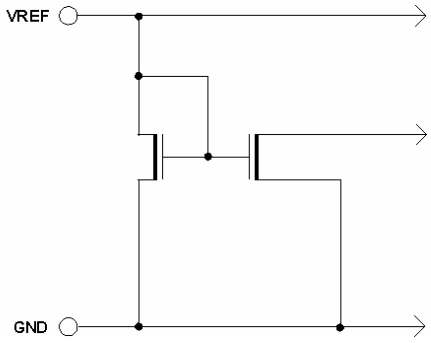

Figure 7 – VREF circuit.

Signal Description

HIGH SPEED INPUT CLOCK.

The RDA012LP DAC high-speed clock input is differential and can be driven from typical LVPECL circuits. Also a differential sinusoidal clock can be used. The CLKIP and CLKIN inputs are internally terminated with 50Ω to VTT which should be connected to a well decoupled 1.3V supply when used with a LVPECL signal source. VTT should be terminated to 2.0V if the CLKI connection is AC coupled (Figure 8). Since the DAC's output phase noise is directly related to the input clock noise and jitter, a low-jitter clock source is ideal. The internal clock driver generates very little added jitter (~100fs).

DATA INPUT.

The data inputs are single ended LVPECL compatible. VECL is used as a voltage reference for the data input buffers.

ANALOG OUTPUT.

The outputs OUTP and OUTN should both be connected though a 50Ω resistor to VCC. This will give a full-scale amplitude of 0.3 volt (both outputs must be terminated), 0.6 volt differentially. The output common mode can be changed by terminating the load resistors to a different voltage.

REFERENCE.

VREF pin supplies the reference voltage for the DAC core and is recommended that an accurate, temperature-compensated voltage reference be used. The output full-scale voltage follows the relationship $V_{FS} = 0.3xV_{REF}$. Note that the RDA012LP DAC is optimized to have the best performance with a reference voltage of 1.3V. The output resistance of the reference node is 560 Ω ±10%.

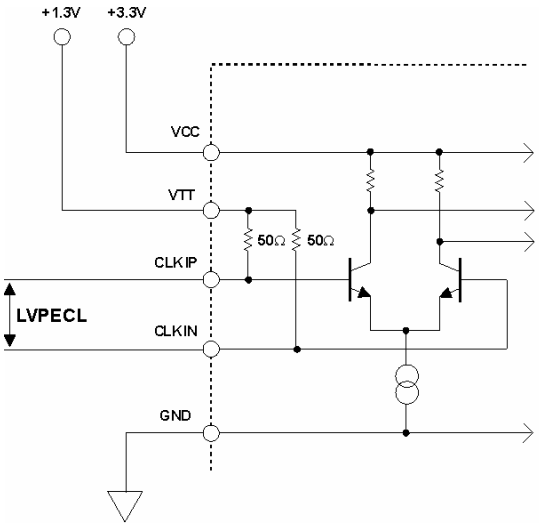

Figure 8 – LVPECL clock.

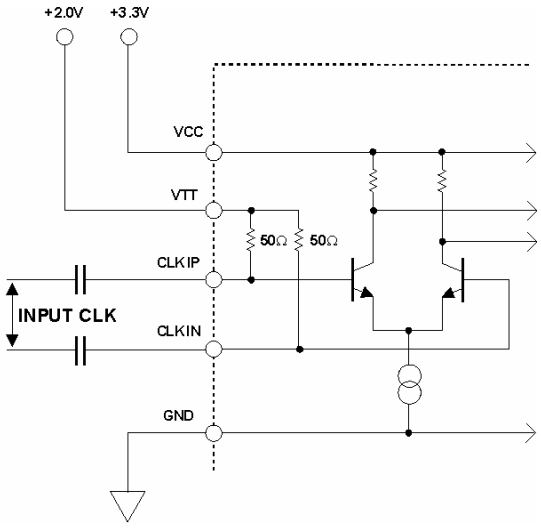

Figure 9 – AC coupled clock.

Typical Operating Circuit

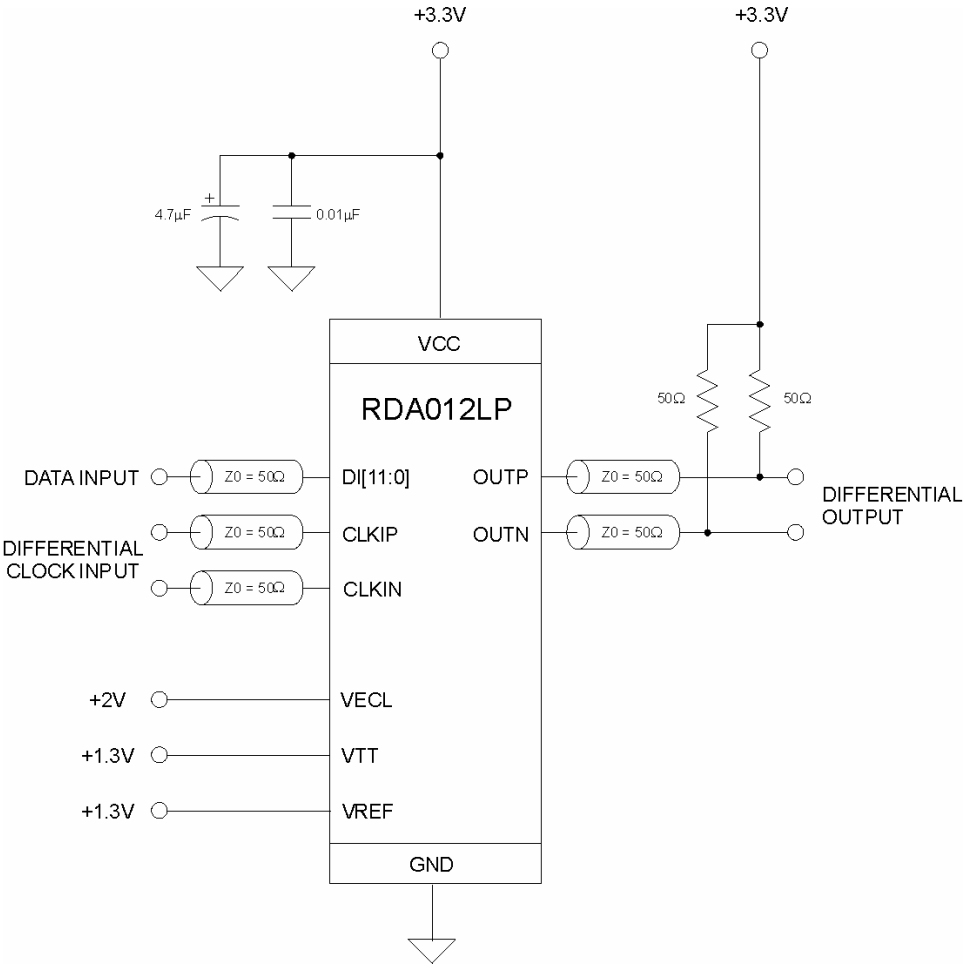

Figure 10 - RDA012LP typical operating circuit using external voltage reference.

Typical Performance

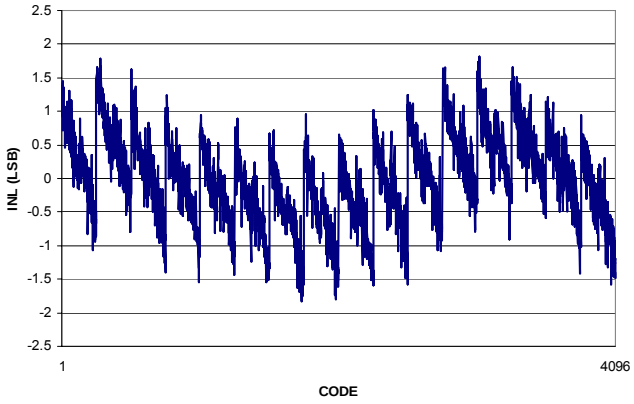

Figure 11 - Integral non-linearity.

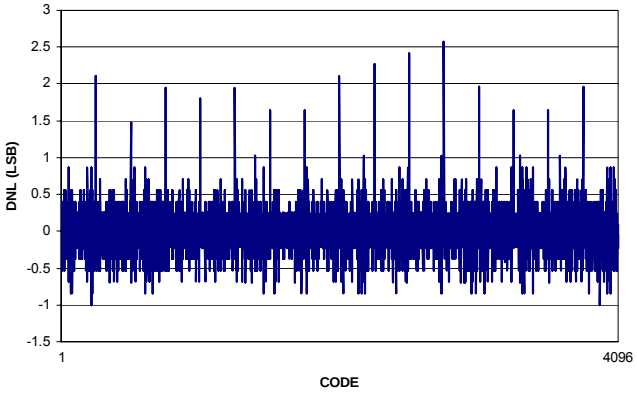

Figure 12 - Differential non-linearity.

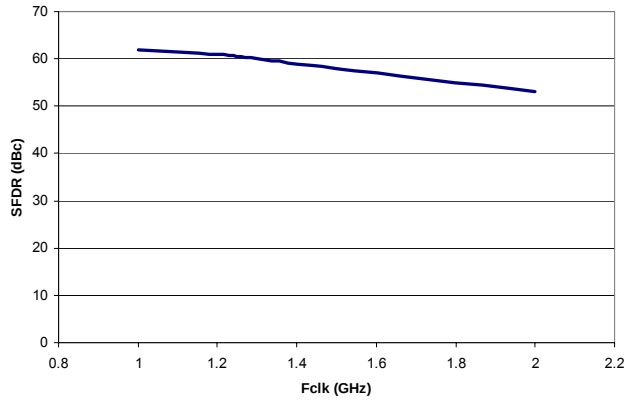

Figure 13 - SFDR for Fout = 1/3 Fclk.

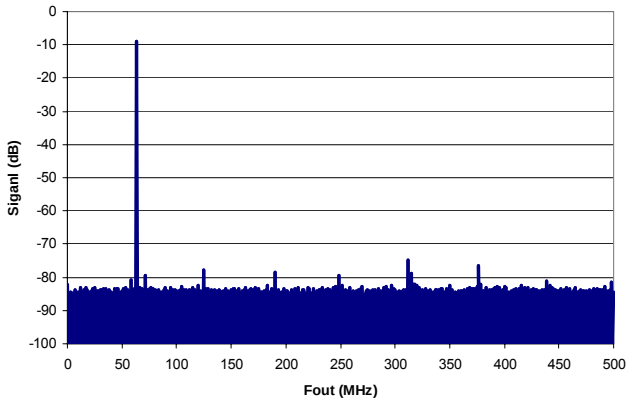

Figure 14 - Spectrum for Fclk=1GHz, Fout=63MHz.

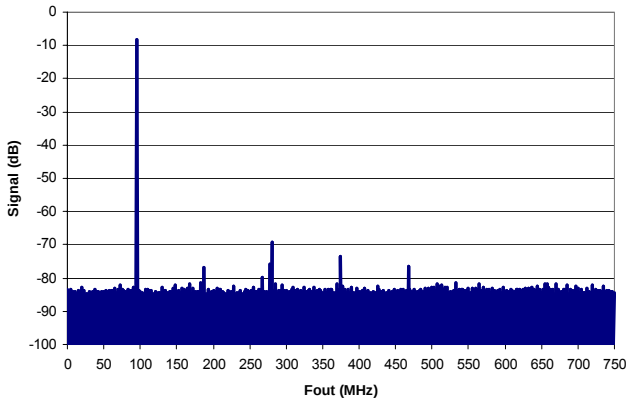

Figure 15 - Spectrum for Fclk=1.5GHz, Fout=95MHz.

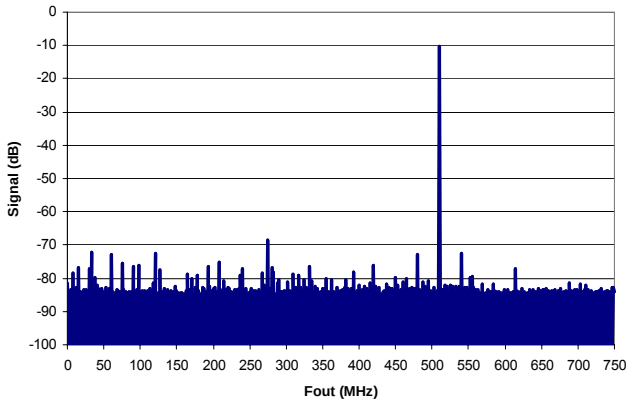

Figure 16 - Spectrum for Fclk=1.5GHz, Fout=510MHz.

Package Information

The package is a 32 lead metal ceramic base, glass sidewall Quad Flat Pack (QFP) with a heat sink slug on the package's bottom. The leads are gull-winged formed. The thermal impedance (junction to base) is approximately 15 °C/W.

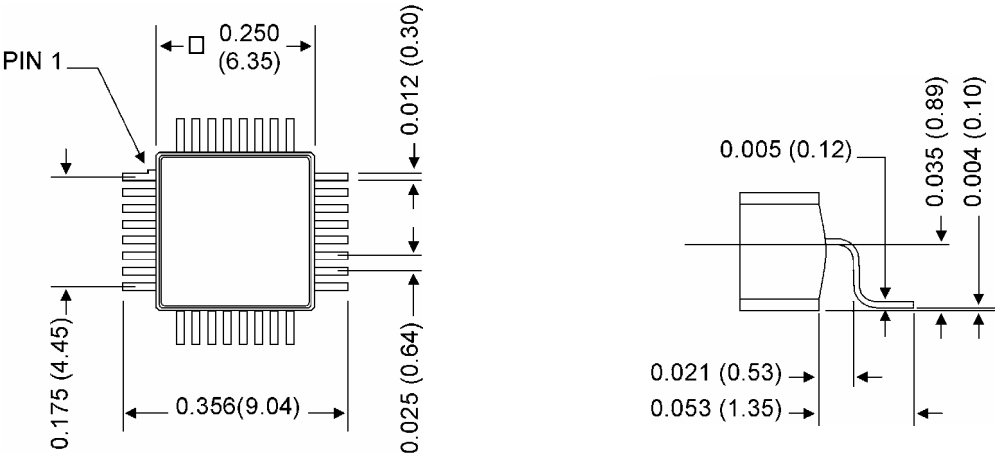

Figure 17 - RDA012LP-QP package, dimensions shown in inches (mm).

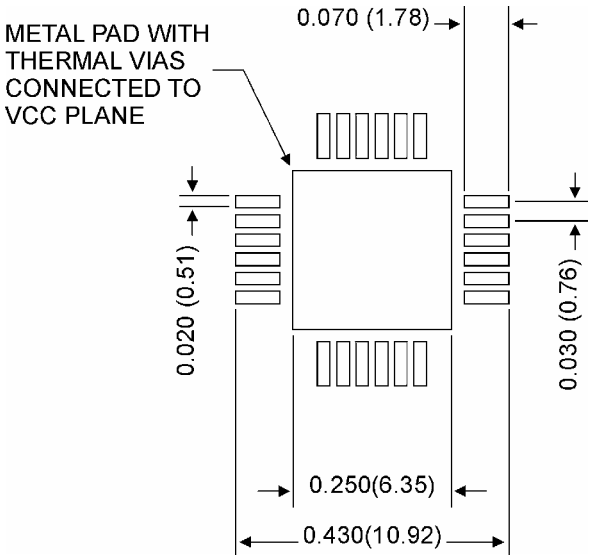

Figure 18 - RDA012LP-QP footprint, dimensions shown in inches (mm).