TELEDYNE SCIENTIFIC COMPANY

RDA112M4MSLPD

12 Bit 2.0 GS/s Low Power Master-Slave Differential 4:1 MUXDAC

Features

- 12 Bit Resolution
- 2.0 GS/s Sampling Rate
- 4:1 or 2:1 Multiplexed Data Input LVDS Compatible
- Divided by 2, 4 or Divided by 8 Clock Out (DDR Support)
- Master-Slave Mode for Synchronous Operation (Multiple Devices)
- Differential Analog Output
- Adjustable Output Signal: Up to 600mV (single-ended)
- Offset Binary Input Code Format
- DNL: ±2 LSB Typical
- INL: ±2 LSB Typical
- 3.3V Power Supply, 2.5V for Input Signals
- 1.1W Power Dissipation Typical
- 224 Balls BGA Package

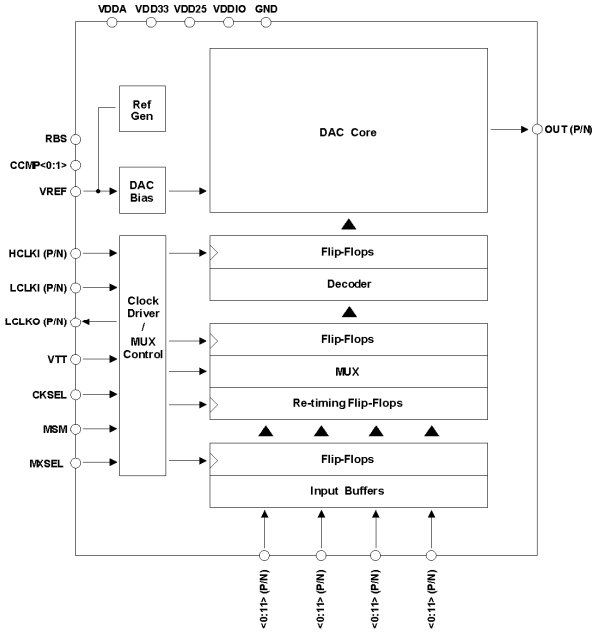

Figure 1 - Functional Block Diagram

Product Description

The RDA112M4MSLPD is a low-power 12 bit digital to analog converter (DAC) with a data sampling rate of 2.0GS/s. It has been optimized for applications demanding a high performance low-power DAC, achieving more than 50 dBc of spurious free dynamic range (SFDR) at 2 GS/s with f_{out} of 667 MHz. Interface to the DAC is made easy by its multiplexer (in 4:1 or 2:1 mode), allowing direct connection to a FPGA or ASIC with no extra components. The DAC utilizes a segmented current source to reduce glitch energy and achieve high linearity performance. For better dynamic performance, the DAC outputs are internally terminated with 50Ω resistors. It outputs a nominally 300mVpp signal when terminated with external 50Ω resistors.

Ordering information

PART NUMBER	DESCRIPTION
RDA112M4MSLPD-DI	12 BIT 2.0GS/s MUXDAC, DIE
RDA112M4MSLPD-BG	12 BIT 2.0GS/s MUXDAC, BGA Package
EVRDA112M4MSLPD-BG	RDA112M4MSLPD-BG Evaluation Board

CAUTION
DEVICE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

Absolute Maximum Ratings

Supply Voltages

Between GNDs ..... -0.3V to 0.3V
Between VDDA and VDD33..... -0.3V to 0.3V
VDDA, VDD33 to GND .....0V to 3.8V
VDD25 to GND .....0V to 2.9V

RF Input Voltages

HCLKIP, HCLKIN to GND ..... 0V to VDD33
LCLKIP, LCLKIN to GND ..... 0V to VDD33

HS Digital Input Voltages

DIA<0:11> (P/N) ..... 0V to VDDIO
DIB<0:11> (P/N) ..... 0V to VDDIO
DIC<0:11> (P/N) ..... 0V to VDDIO
DID<0:11> (P/N) ..... 0V to VDDIO

Output Termination Voltages

OUTP, OUTN to GND..... 0V to VDDA+1V

Temperature

Case Temperature.....-15 to 85 °C
Junction Temperature..... 120 °C
Storage..... -40 to 125 °C

DC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VDDA = 3.3V; VDD33 = 3.3V; VDD25 = 2.5V; VDDIO = 2.5V; VTT = 1.3V; VREF = 1.2V; MSM = master; MXSEL = 4:1; RBS = 1K6Ω; Clock: 2GHz, 0.6Vpp Differential; Outputs Terminated into 50Ω to 3.3V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
1.0	**DC TRANSFER FUNCTION**						
1.1	Differential Nonlinearity	DNL	Maximum of Absolute Value		2		LSB
1.2	Integral Nonlinearity	INL	Maximum of Absolute Value		2		LSB
2.0	**TEMPERATURE DRIFT**						
2.1	Warm-up Time		After Power-up			30	s
3.0	**HIGH CLOCK INPUT (HCLKIP, HCLKIN)**						
3.1	Input Resistance	R_{CLKI}	Resistance (HCLKI P/N) to VTT		50		Ω
3.2	Input Capacitance	C_{CLKI}			500		fF
4.0	**LOW CLOCK INPUT (LCLKIP, LCLKIN)**						
4.1	Input Resistance	R_{LCLKI}	Resistance from LCLKIP to LCLKIN		100		Ω
4.2	Input Capacitance	C_{LCLKI}			500		fF
5.0	**LOW CLOCK OUTPUT (LCLKOP, LCLKON)**						
5.1	Amplitude	$V_{CPP,LCLKO}$	LCLKO P/N Terminated into 100Ω		400		mVpp
5.2	Common Mode Voltage	$V_{CM,LCLKO}$			1200		mV
6.0	**DIGITAL INPUTS (DIA<0:11>(P/N), DIB<0:11>(P/N), DIC<0:11>(P/N), DID<0:11>(P/N))**						
6.1	Input Resistance	R_{DIN}	Differential (from DI<N>P to DI<N>N)		100		Ω
6.2	Input Capacitance	C_{DIN}			500		fF
7.0	**ANALOG OUTPUTS (OUTP, OUTN)**						
7.1	Full-scale Output Swing	V_{FSD}	Differential, Terminated Into 50Ω to VDD=3.3V on Each Output		600	1200	mVpp
7.2	Full-scale Output Swing	V_{FSS}	Single Ended, Terminated Into 50Ω to VDD=3.3V		300	600	mVpp
7.3	Full-scale Output Range	V_{FSRS}	Single Ended, Terminated Into 50Ω to VDD=3.3V (MIN=000h, MAX=FFFh)	2.7		3.3	Vpp
7.4	Output Current	I_{OUT}	Terminated Into 50Ω to VDD=3.3V		6.3		mA
8.0	**REFERENCE (VREF)**						
8.1	Reference Voltage	V_{VREF}	Output from Internal Reference		1.2		V
9.0	**POWER SUPPLY REQUIREMENTS**						
9.1	Analog Current	IDDA			50		mA
9.2	Digital Current	IDD33			180		mA
9.3	Digital Current	IDD25			85		mA
9.4	I/O Current	IDDIO			70		mA
9.5	Power Dissipation	P			1150		mW

AC Electrical Specification

Test Conditions (see notes for specific conditions): Room Temperature; VDDA = 3.3V; VDD33 = 3.3V; VDD25 = 2.5V; VDDIO = 2.5V; VTT = 1.3V; VREF = 1.2V; MSM = master; MXSEL = 4:1; RBS = 1K6Ω; Clock: 2GHz, 0.6Vpp Differential; Outputs Terminated into 50Ω to 3.3V.

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
10.0	**DYNAMIC PERFORMANCE**						
10.1	Spurious Free Dynamic Range (Single Ended Output)	SFDR 1	F_{CLK} = 1000MHz, F_{OUT} = 20MHz		70		dBc
10.2		SFDR 2	F_{CLK} = 1000MHz, F_{OUT} = 250MHz		67		dBc
10.3		SFDR 3	F_{CLK} = 1000MHz, F_{OUT} = 333MHz		60		dBc
10.4		SFDR 4	F_{CLK} = 1000MHz, F_{OUT} = 480MHz		61		dBc
10.5		SFDR 5	F_{CLK} = 1500MHz, F_{OUT} = 30MHz		67		dBc
10.6		SFDR 6	F_{CLK} = 1500MHz, F_{OUT} = 370MHz		64		dBc
10.7		SFDR 7	F_{CLK} = 1500MHz, F_{OUT} = 500MHz		61		dBc
10.8		SFDR 8	F_{CLK} = 1500MHz, F_{OUT} = 720MHz		52		dBc
10.9		SFDR 9	F_{CLK} = 2000MHz, F_{OUT} = 40MHz		62		dBc
10.10		SFDR 10	F_{CLK} = 2000MHz, F_{OUT} = 500MHz		53		dBc
10.11		SFDR 11	F_{CLK} = 2000MHz, F_{OUT} = 666MHz		52		dBc
10.12		SFDR 12	F_{CLK} = 2000MHz, F_{OUT} = 960MHz		45		dBc
10.13	Clock Feedthrough	FD			-40		dBc
11.0	**LOW CLOCK OUTPUT (LCLKOP, LCLKON)**						
11.1	Delay	$T_{LCDLY,HCLKI}$	Propagation Delay HCLKI to LCLKO	410		630	ps
12.0	**ANALOG OUTPUTS (OUTP, OUTN)**						
12.1	Rise Time	$T_{R,OUT}$			400		ps
12.2	Fall Time	$T_{F,OUT}$			400		ps

Operating Conditions

	PARAMETER	SYMBOL	CONDITIONS, NOTE	MIN	TYP	MAX	UNITS
13.0	**HIGH CLOCK INPUT (HCLKIP, HCLKIN)**						
13.1	Amplitude	$V_{CPP,HCLKI}$		200		1000	mVpp
13.2	Common Mode Voltage	$V_{CCM,HCLKI}$		2000		2800	mV
13.3	Maximum Frequency	$F_{MAX,HCLKI}$		2000			MHz
13.4	Minimum Frequency	$F_{MIN,HCLKI}$				1	MHz
14.0	**LOW CLOCK INPUT (LCLKIP, LCLKIN)**						
14.1	Amplitude	$V_{CPP,LCLKI}$		200		1000	mVpp
14.2	Common Mode Voltage	$V_{CCM,LCLKI}$		500		VDDIO-500	mV
14.3	Setup Time	$T_{LCSET,HCLKI}$	Setup Time LCLKI to HCLKI	600			ps
14.4	Hold Time	$T_{LCHLD,HCLKI}$	Hold Time LCLKI to HCLKI	-270			ps
15.0	**DIGITAL INPUTS (MSM, MXSEL, CLKSEL, DLSEL<0:1>)**						
15.1	Input High Voltage	$V_{IH,CTRI}$		VDDIO-500		VDDIO	mV
15.2	Input Low Voltage	$V_{IL,CTRI}$		0		0.5	V
16.0	**DIGITAL INPUTS (DIA<0:11>(P/N), DIB<0:11>(P/N), DIC<0:11>(P/N), DID<0:11>(P/N))**						
16.1	Amplitude	$V_{CPP,DI}$		200		1000	mVpp
16.2	Common Mode Voltage	$V_{CCM,DI}$		500		VDDIO-500	mV
16.3	Setup Time	$T_{DISET,LCLKO}$	Setup Time DI to LCLKO	650			ps
16.4	Hold Time	$T_{DIHLD,LCLKO}$	Hold Time DI to LCLKO	-300			ps
17.0	**TERMINATION VOLTAGE (VTT) [1] (note 1)**						
17.1	Termination Voltage	V_{TT}	Termination Voltage for HCLKI		1.3		V
18.0	**REFERENCE VOLTAGE (VREF)[2] (note 2)**						
18.1	Reference Voltage	V_{REF}			1.2		V
19.0	**POWER SUPPLY REQUIREMENTS**						
19.1	Analog Supply Voltage	VDDA		3.1	3.3	3.5	V
19.2	Digital Supply Voltage	VDD33		3.1	3.3	3.5	V
19.3	Digital Supply Voltage	VDD25		2.3	2.5	2.7	V
19.4	I/O Supply Voltage	VDDIO		2.3	2.5	2.7	V
20.0	**OPERATING TEMPERATURE[3] (note 3)**						
20.1	Case Temperature	Tc				85	°C
20.2	Junction Temperature	Tj				120	°C

[1] The termination voltage of 1.3V is to be used if the HCLKI source is a LVPECL driver in a DC coupled connection. If the HCLKI source is AC coupled VTT should be 2V.

[2] The DAC core current is generated from an internal reference that is both temperature and supply dependent. The Internal reference can change up to ±2% by changing the supply voltage within the specified range. It can also change up to ±5% according to operating temperature changes. The change in temperature and supply can be minimized by using a precision external voltage reference source connected to VREF.

[3] The part is designed to function within a junction temperature range of -40 ~ 120°C. For the best performance, operation within the specified temperature range with a proper heatsink attached to the device is recommended.

Pin Description

P/I/O	PIN	NUM.	NAME	FUNCTION
P	B3, B9, B10, B13, B14, C5, C6, C7, C8,C9, C10, C11, C12, C13, C14, C15	16	VDDA	Analog Power Supply
P	E3, F3, F16, G16	4	VDD33	Digital Power Supply, 3.3V
P	A2, F1, G18	3	VDD25	Digital Power Supply, 2.5V
P	G1, G3, K1, K3, K16, K18, N1, N3, N16, N18, T1, T3, T9, T10, T16, T18	16	VDDIO	I/O Power Supply
P	A6, A7, A9, A10, A13, B5, B6, B7, B8, B11, B12, B15, B16, C1, C4, D2, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, E2, E4, F2, F4, F15, F17, F18, G2, G4, G15, G17, K2, K4, K15, K17, N2, N4, N15, N17, R9, R10, T2, T4, T15, T17	52	GND	Ground
I	B4	1	RBS	External Resistor for Bias Reference
I	A3, A4	2	CCMP(P/N)	External Compensation Capacitor
I	A5	1	VREF	1.2V External Reference Voltage
I	D3	1	VTT	HCLKI Termination Voltage
I	C2	1	CLKSEL	Low Clock Selection: High DDR Low SDR
I	B2, B1	2	DSEL<0:1>	Clock Delay Selection: 0 – 1 HCLK Delay 1 – 2 HCLK Delay 2 – 3 HCLK Delay 3 – 4 HCLK Delay
I	C3	1	MSM	Master Slave Selection: High Slave Low Master
I	A1	1	MXSEL	Multiplexer Selection: High 2:1 Channel AD Low 4:1 Channel ABCD
I	E1	1	HCLKIP	High Clock Input
I	D1	1	HCLKIN	
I	H15, L15, P15, U18, R14, R12, R8, R6, U4, R4, M4, J4	12	A<0:11>P	A<i> Is Channel A Digital Bit i Input. MSB is bit 11.
I	H16, L16, P16, V18, T14, T12, T8, T6, V4, R3, M3, J3	12	A<0:11>N	
I	J15, M15, R15, U17, R13, R11, R7, R5, U3, P4, L4, H4	12	B<0:11>P	B<i> Is Channel B Digital Bit i Input. MSB is bit 11.
I	J16, M16, R16, V17, T13, T11, T7, T5, V3, P3, L3, H3	12	B<0:11>N	
I	H17, L17, P17,U16, U14, U12, U8, U6, U2, R2, M2, J2	12	C<0:11>P	C<i> Is Channel C Digital Bit i Input. MSB is bit 11.
I	H18, L18, P18, V16, V14, V12, V8, V6, V2, R1, M1, J1	12	C<0:11>N	
I	J17, M17, R17, U15, U13, U11, U7, U5, V1, P2, L2, H2	12	D<0:11>P	D<i> Is Channel D Digital Bit i Input. MSB is bit 11.
I	J18, M18, R18, V15, V13, V11, V7, V5, U1, P1, L1, H1	12	D<0:11>N	
I	U9	1	LCLKIP	Low Clock Input
I	V9	1	LCLKIN	
O	U10	1	LCLKOP	Low Clock Output
O	V10	1	LCLKON	
O	A12	1	OUTP	Differential Output
O	A11	1	OUTN	
R	A8, A14, A15, A16, A17, A18, B17, B18, C16, C17, C18, D15, D16, D17, D18, E15, E16, E17, E18	19	RES	Reserved

Pin Layout (TOP view)

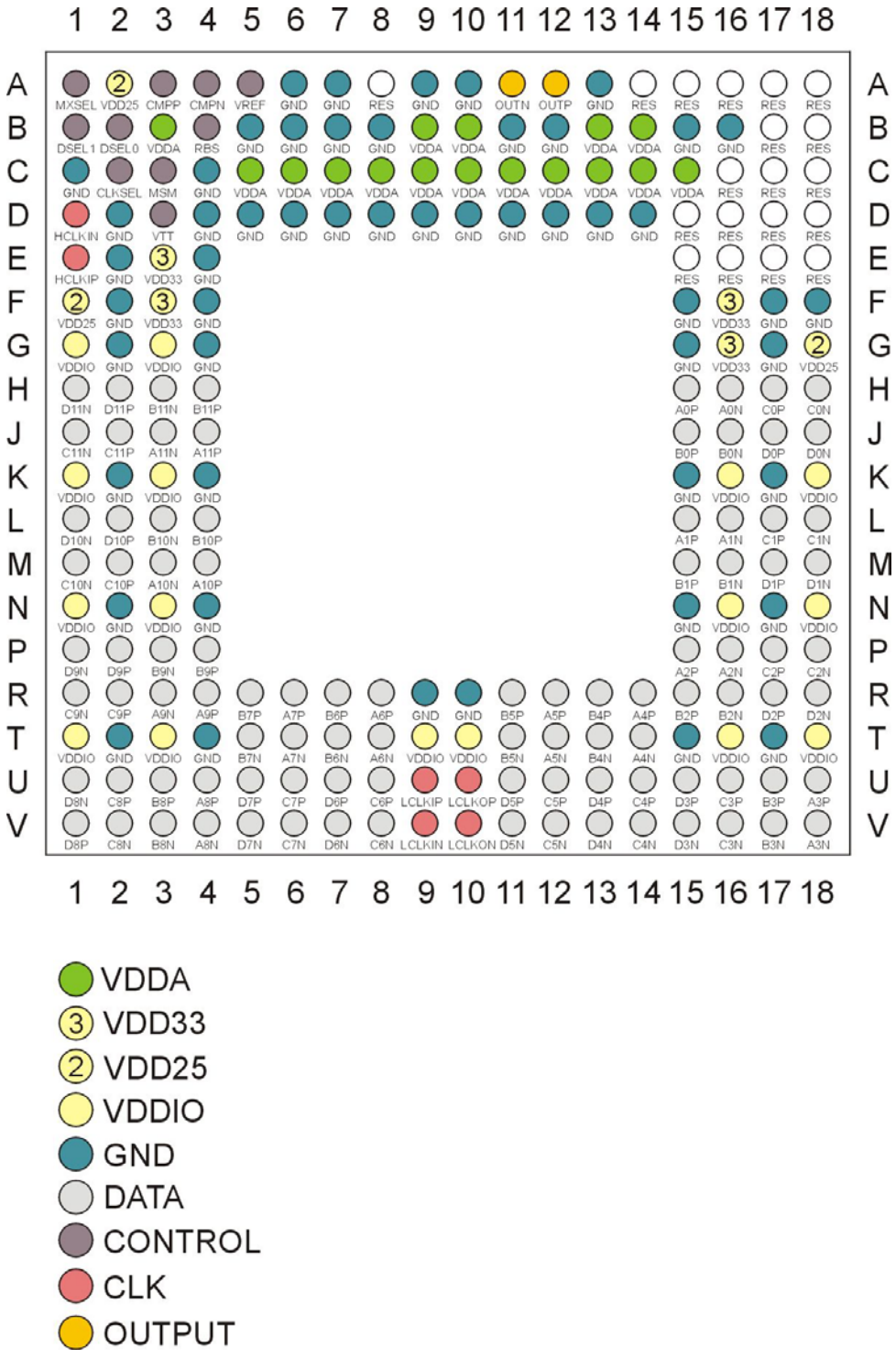

Figure 2 - RDA112M4MSLPD pinout. (top view)

Typical Operating Circuit

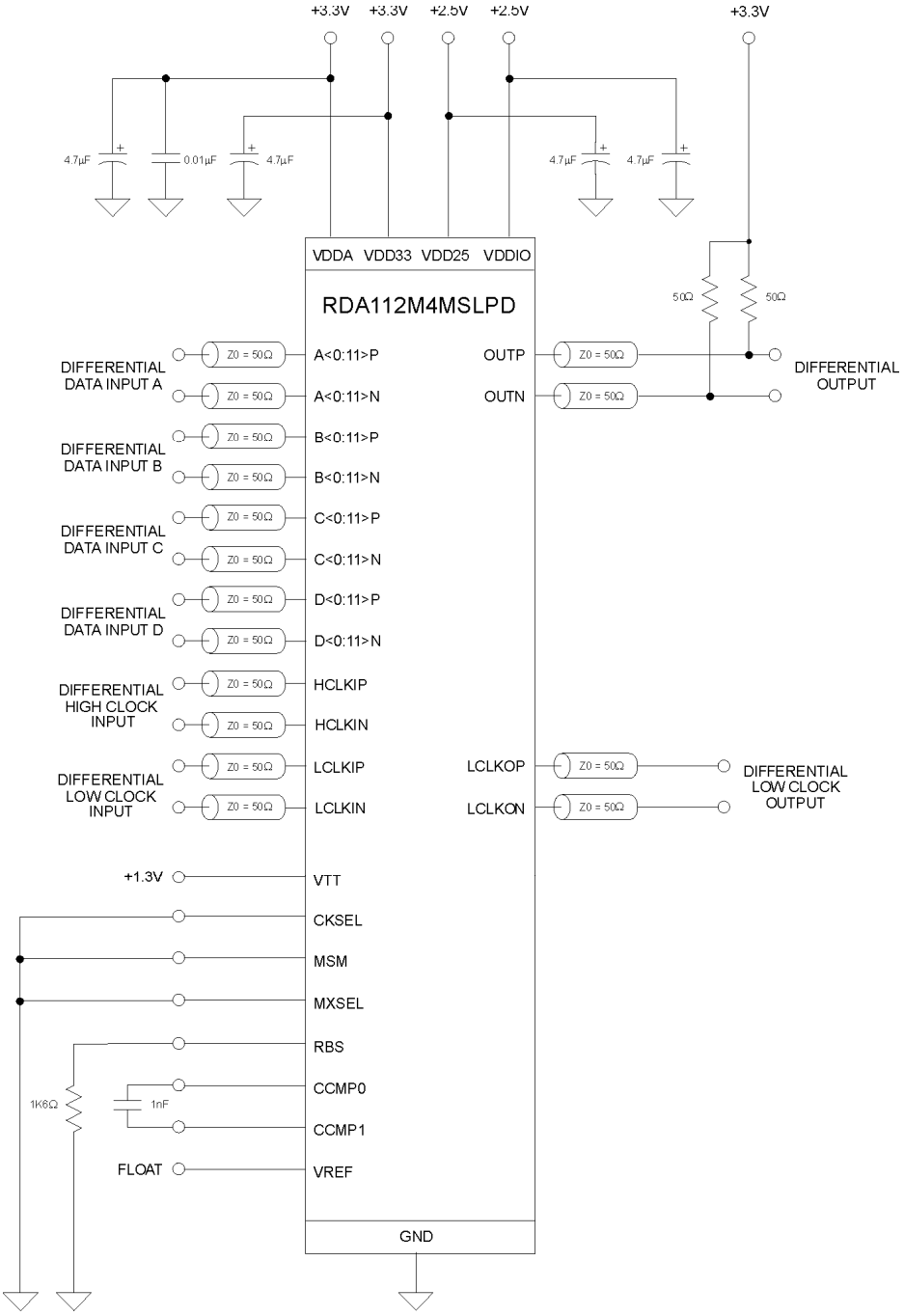

Figure 3 - RDA112M4MSLPD typical operating circuit, single device, SDR output clock, using internal voltage reference.

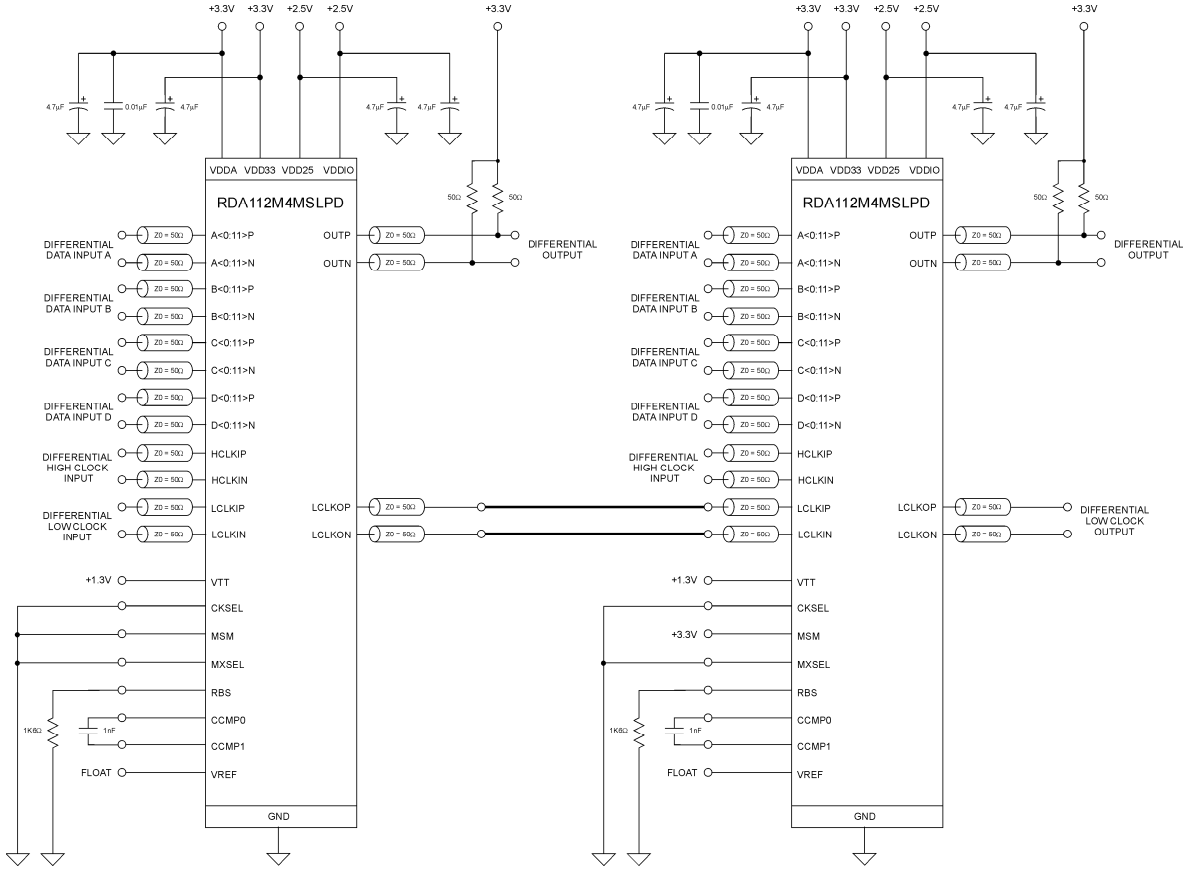

Figure 4 - RDA112M4MSLPD typical operating circuit in master-slave configuration.

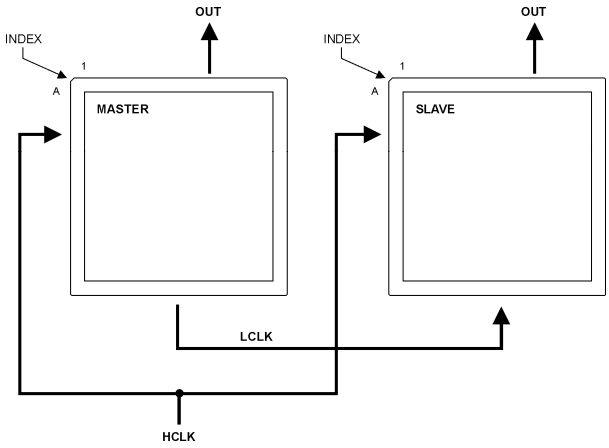

Figure 5 - RDA112M4MSLPD placement in master-slave configuration.

Equivalent Circuit

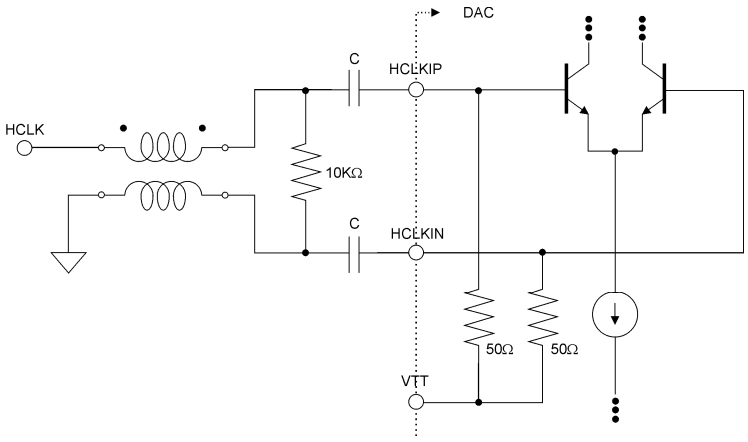

Figure 6 - RDA112M4MSLPD high speed clock input circuit (HCLKI), showing a single ended clock source. The clock common mode is set by VTT (which in an AC coupled clock configuration is 2V).

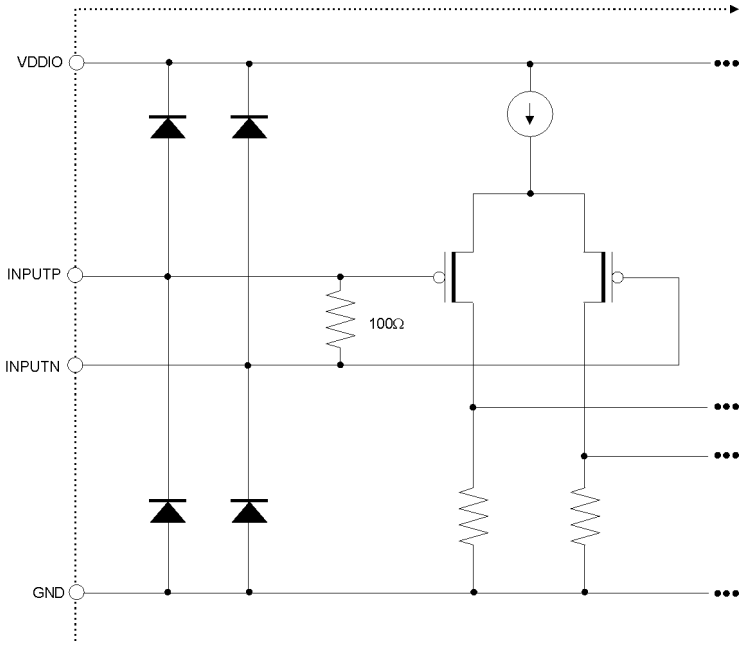

Figure 7 - RDA112M4MSLPD low speed clock input (LCLKI) and data in input (DI<A,B,C,D>) circuit.

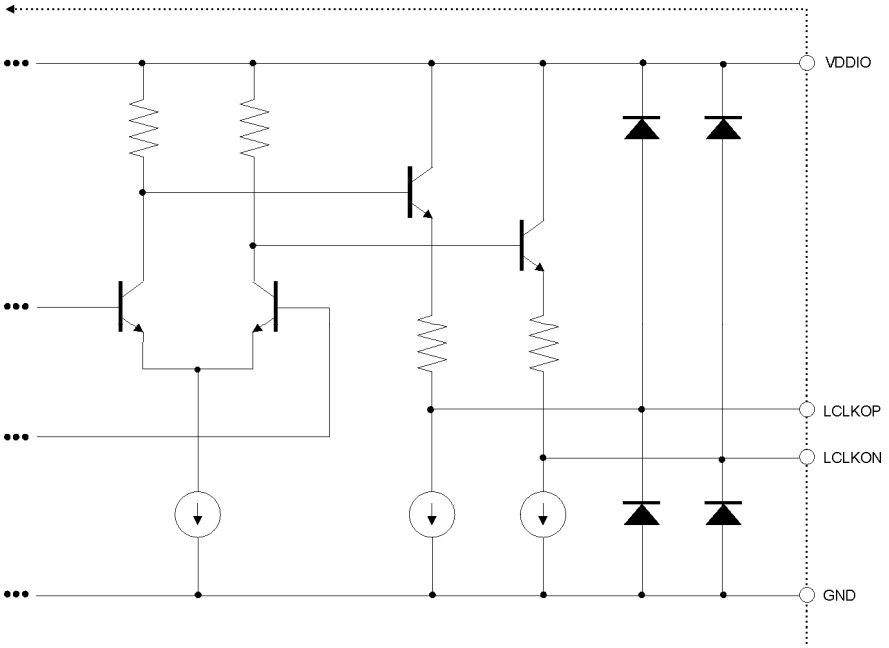

Figure 8 - RDA112M4MSLPD low speed clock output (LCLKO) circuit.

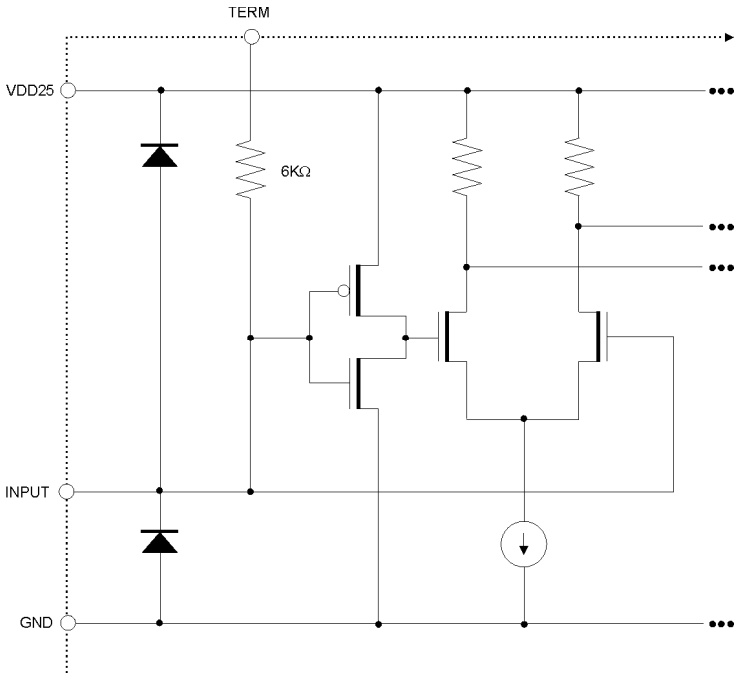

Figure 9 - RDA112M4MSLPD control input (CKSEL, DSEL<0:1>, MSM, MXSEL) circuit. Term is internally connected to GND except if the input is CLKSEL, in which case Term is connected to VDD25.

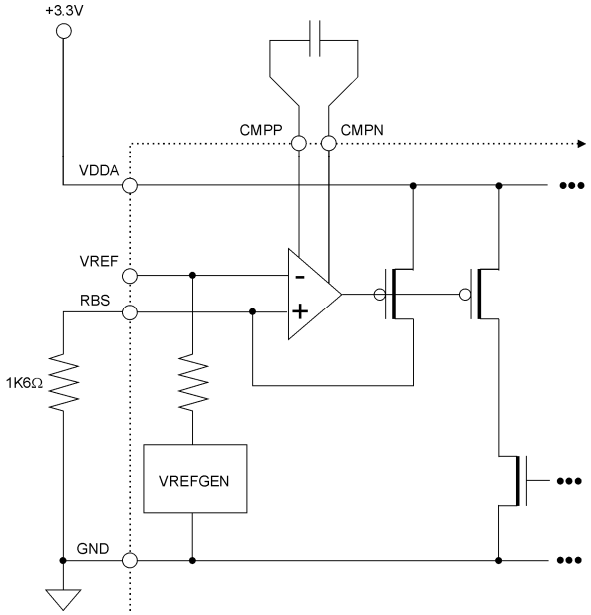

Figure 10 - RDA112M4MSLPD voltage reference circuit.

Typical Performance

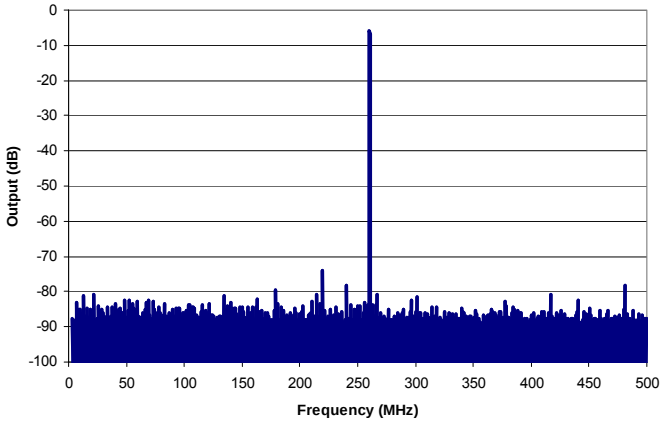

Figure 11 – Spectrum for F_{CLK}=1GHz, F_{OUT}=260MHz.

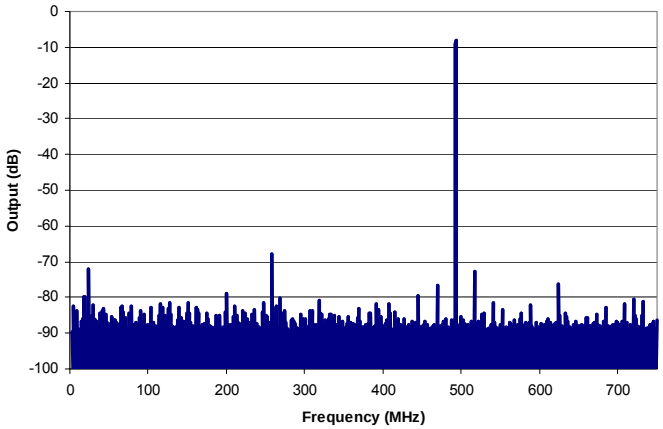

Figure 12 – Spectrum for F_{CLK}=1.5GHz, F_{OUT}=490MHz.

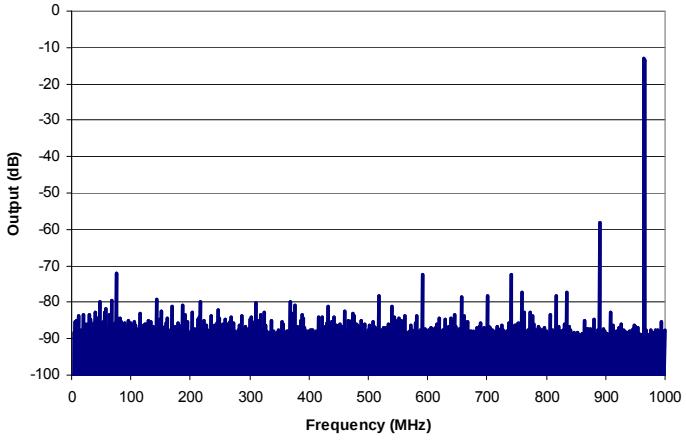

Figure 13 – Spectrum for F_{CLK}=2GHz, F_{OUT}=960MHz.

Package Information

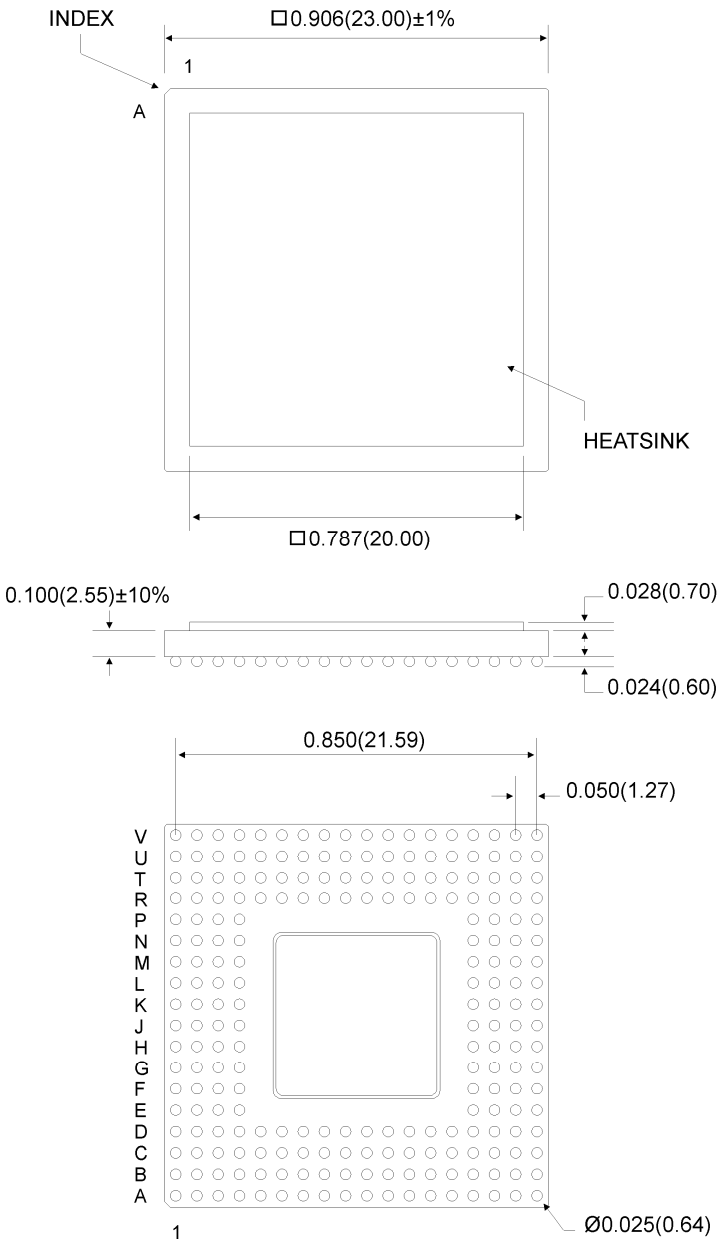

Figure 14 - RDA112M4MSLPD-BG package, dimensions shown in inches (mm).