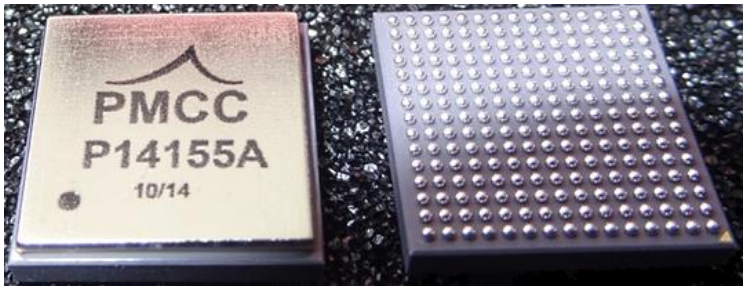
P14155A: SAR Rx Signal Processing ASIC Datasheet Rev 2.2

Pacific MicroCHIP Corp.

SUMMARY



P14155A is a SAR Rx Signal Processing ASIC, featuring 128 RF (5 - 500MHz) analog signal processing, independent digitizing of each input (2-bit 1GS/s) and digital cross-correlation. Cross-correlation results in 4096 products plus 512 totalizer values from digitizers. Each input channel uses a variable gain amplifier (VGA) coupled with a programmable automatic gain control (AGC) loop to keep the ratio of the digitizer comparators thresholds at the predefined constant level, independent from the input signal levels, which can vary within -20…-10dBm. Integration time of the cross-correlation results is programmable. Since each cross-correlator's cell contains a 26-bit depth accumulator, the maximum supported integration time is 11ms. The ASIC operates in two phases controlled by the outside host: integration and data readout. During the first phase, the ASIC performs input signals cross-correlation for the pre-programmed period. During the second phase, the ASIC transmits correlation results via 8-bit output bus. Readout speed is programmable and the entire correlation result can be read in 0.11…2.3 millisecond. The ASIC consumes 1.7W during correlation and 0.33W during readout from 1.0V and 1.8V supplies.

A block diagram of the ASIC is shown on Figure 1. Analog signals from inputs ARM1 and ARM2 with a bandwidth from 5 MHz to 500 MHz go through VGA to the 2-bit ADC. The AGC circuit using 2-bit data adjusts the input signal level at the ADC input through the VGA. The VGA gain is controlled so that the average duty cycle value of LSB ADC output would be 0.7 by default.

Data from the ADC comes to the main functional block of the ASIC – the Cross-Correlation Matrix. This block is responsible for cross-correlation of 64 2-bit signals from one arm (array of receivers) and 64 2-bit signals from another arm. The matrix consists of 4096 cross-correlation cells, 64 vertical totalizers and 64 horizontal totalizers. The cross-correlation cell (XCC) consists of the multiplication and accumulation blocks. Power consumption of a single correlation cell is minimized. The totalizer is an array of adder's cells which count the number of occurrences of each possible two-bit input values from the ADC. An Output Multiplexer (MUX) is a serializer of the values stored in Cross-Correlation Cells and Totalizer Cells. The I^2C Interface is used for the ASIC's control. Built-in self-test (BIST) is used for the testing of a device's digital correlator matrix.

FEATURES

- 64x2 single-ended inputs with on-chip termination,
- Computed correlation of a pair of two-bit inputs, "a" and "b":
  a, b ∈ {-3, -1, 1, 3}
  a×b ⇒ {-9, -3, -1, 1, 3, 9}
  ÷ 3 ⇒ {-3, -1, 0, 0, 1, 3}
  + 3 ⇒ {0, 2, 3, 3, 4, 6}
- 1 GHz clock signal for 2-bit ADC,
- Input clock delay adjustment circuit,
- 5MHz to 500MHz input signal frequency range,
- Adjustable VGA input termination 50Ω/100Ω/200Ω/Hi-Z for parallel chip connection,
- -20dBm to -10dBm input power levels range,
- Zero-crossing comparator offset correction,
- Adjustable ADC conversion range,
- Cross-Correlation cell with a 26-bit depth accumulator,
- Built-in digital totalizers in each channel,
- External clock input for the cross-correlator's matrix readout,
- Programmable integration and reading time,

- Serialized 8-bit output data,
- Tristate output buffer,
- Power per correlation cell is <0.3mW,
- I^2C control interface up to 400kHz ,
- Correlator matrix built-in self-test,
- ESD protection for I/O,
- Radiation hardness through using 45nm SOI CMOS process,
- BGA289 package.

BLOCK DIAGRAM

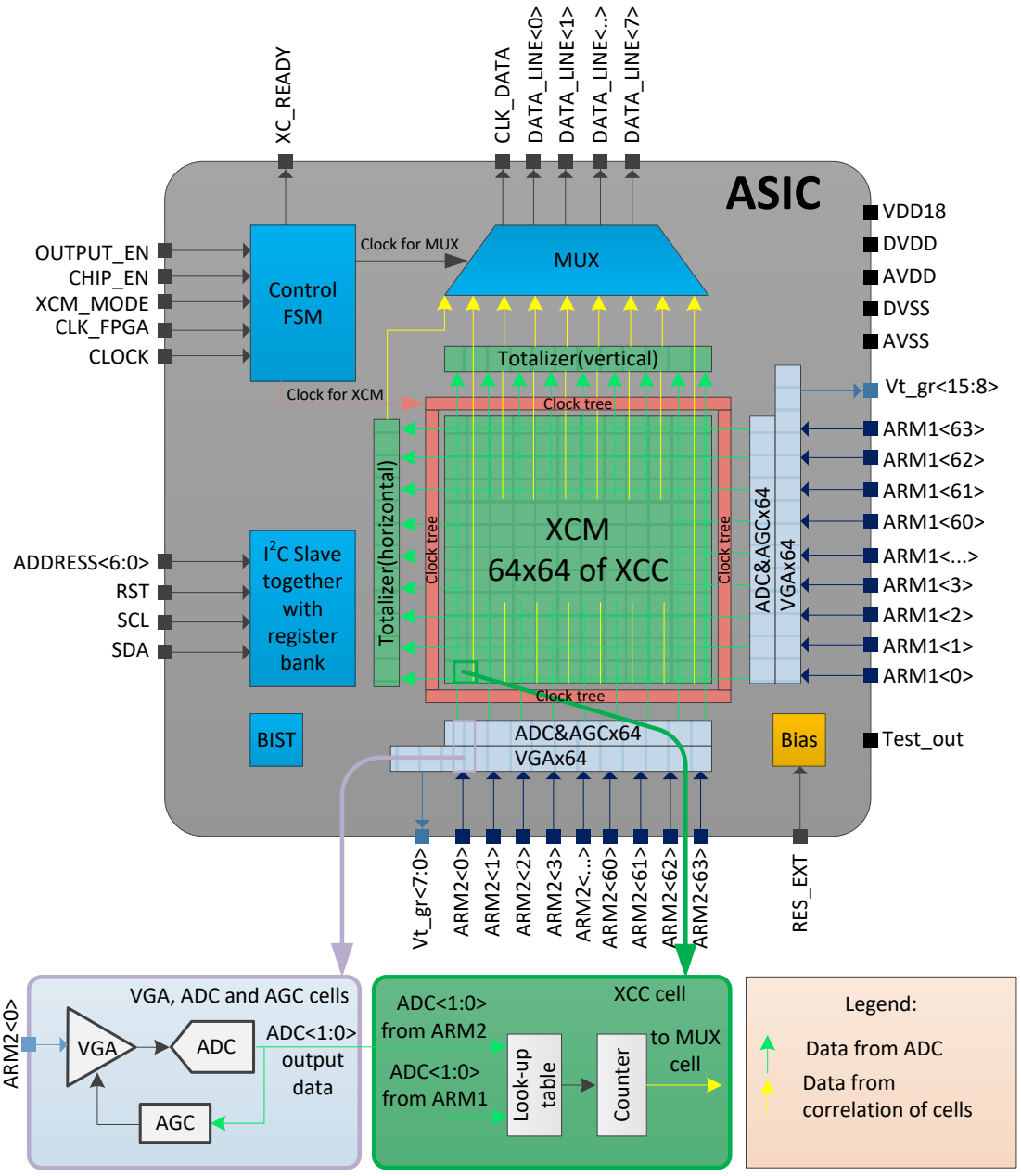


Figure 1. ASIC's Block Diagram

PIN DESCRIPTIONS

Table 1. Pin Descriptions

Name	Pin #	Description	Type
ARM1<63:0>	*	Analog inputs from arm1	AI
ARM2<63:0>	*	Analog inputs from arm2	AI
CLOCK	O15	Input clock 1GHz	AI
XCM_MODE	N14	Correlation array mode (integration or readout)	DI
RES_EXT	C3	External 24.8kOm resistor connection	AI
CLK_FPGA	L14	Input clock from FPGA	AI
ENABLE	N4	Chip enable	DI
OUTPUT_ENABLE	M14	Output state of DATA_LINE<7:0> bus and CLK_DATA output: hi-z mode or CMOS (readout) mode	DI
ADDRESS<6:0>	N5-N11	I2C address line	DI
RST	O9	I2C and ASIC reset line	DI
SCL	N12	I2C serial clock line	DI
SDA	N13	I2C serial data line	DIO
DATA_LINE<7:0>	*	Cross-Correlator output data line	DO
CLK_DATA	I15	Cross-Correlator output clock for reading synchronization	DO
XC_READY	K14	Correlation mode status	DO
VTD_GR<15:0>	*	Input termination center-tap for each VGA group	AO
TEST_PAD	D4	Analog test output	AO
AVDD	*	Analog supply 1.0V	PW
DVDD	*	Digital core supply 1.0V	PW
VDD18	*	Output pads supply 1.8V	PW
DVSS	*	Digital core and output pads ground	GD
AVSS	*	Analog ground	GD

Note: AI – Analog input, DI – digital input, AO – analog output, DO – digital output, DIO – digital input/output, PW – power, GD – ground

* – This data is available in Figure 3.

PACKAGE DRAWING

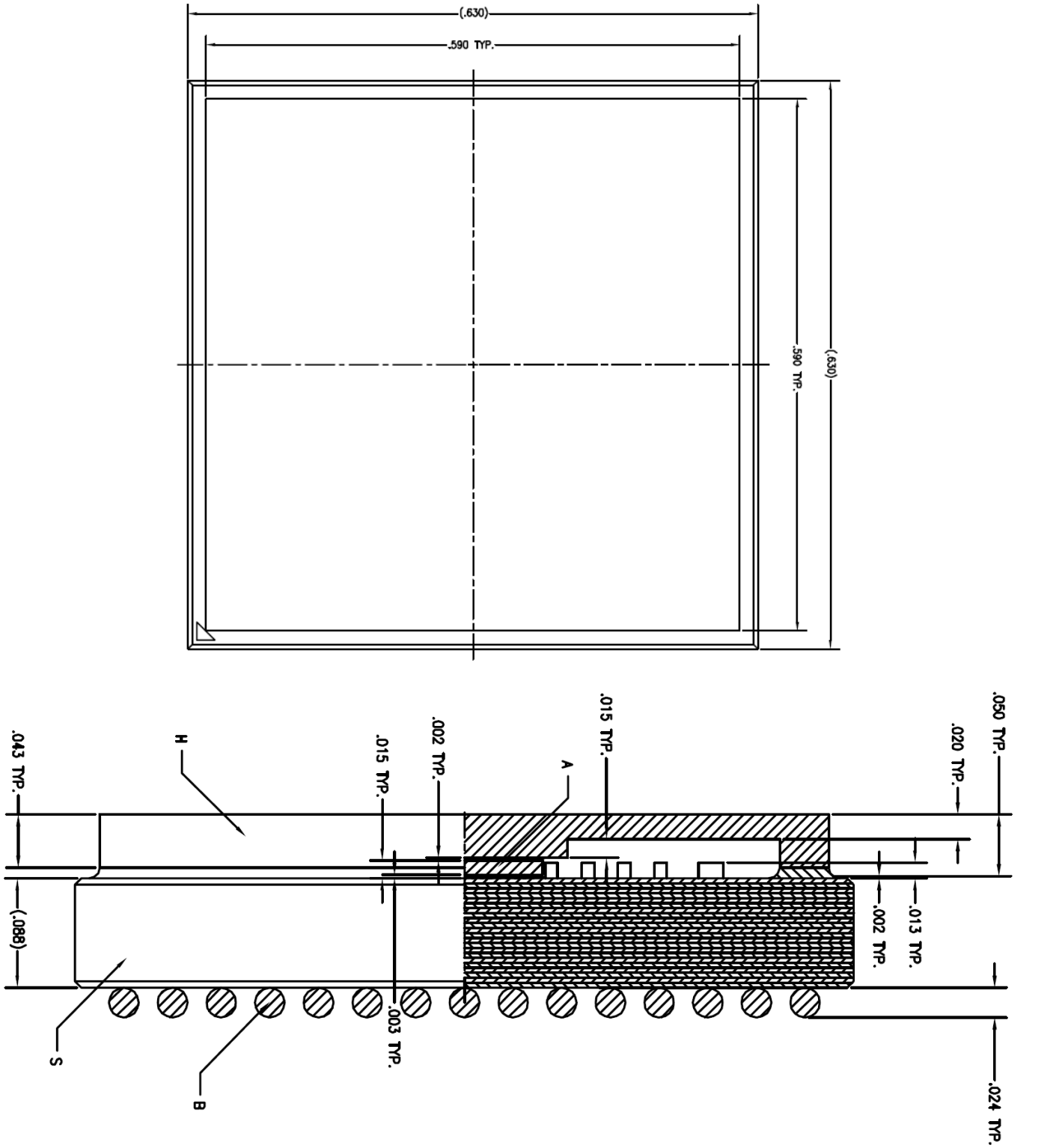


Figure 2. Drawing of the ASIC's package.

PACKAGE BALLS ASSIGNMENT

AVSS	VTD_GR<8>	B4	B10	B16	B22	B28	VTD_GR<12>	B34	B40	B46	B52	B58	VTD_GR<14>	AVSS
VTD_GR<0>	AVDD	AVSS	B8	B14	B20	B26	VTD_GR<10>	B32	B38	B44	B50	VDD18	AVDD	VTD_GR<1>
A4	AVDD	AVSS	B0	B2	B24	B30	DVSS	B36	B42	B56	B62	AVSS	AVDD	A5
A10	A12	A0	AVDD	B6	B12	B18	DVDD	B48	B54	B60	AVDD	A1	A9	A11
A16	A18	A6	A2	AVSS	AVDD	DVSS	DVSS	DVSS	AVDD	AVSS	A7	A3	A15	A17
A22	A24	A20	A8	AVSS	RES_EXT	TEST_PAD	DVDD	ENABLE	ADDRESS<6>	ADDRESS<5>	A13	A25	A21	A23
A28	A30	A26	A14	DVSS	DVDD	DVSS	DVDD	DVSS	ADDRESS<4>	ADDRESS<3>	A19	A31	A27	A29
VTD_GR<2>	VTD_GR<4>	DVSS	DVDD	DVSS	DVDD	DVSS	DVDD	DVDD	ADDRESS<2>	ADDRESS<1>	RST	DVSS	VTD_GR<3>	VTD_GR<5>
A34	A36	A32	A44	DVSS	DVDD	DVSS	DVDD	DVSS	SCL	ADDRESS<0>	A49	A37	A33	A35
A40	A42	A38	A50	DATA_LINE<7>	DATA_LINE<5>	DATA_LINE<3>	DATA_LINE<1>	CLK_FPGA	CLOCK	SDA	A55	A43	A39	A41
A46	A48	A60	A56	DATA_LINE<6>	DATA_LINE<4>	DATA_LINE<2>	DATA_LINE<0>	XC_READY	OUTPUT_ENABLE	XCM_MODE	A61	A57	A45	A47
A52	A54	A62	AVDD	B3	B9	B15	CLK_DATA	B45	B51	B57	AVDD	A63	A51	A53
A58	AVDD	AVSS	B1	B7	B21	B27	DVSS	B33	B39	B61	B63	AVSS	AVDD	A59
VTD_GR<6>	AVDD	VDD18	B13	B19	B25	B31	VTD_GR<13>	B37	B43	B49	B55	AVSS	AVDD	VTD_GR<7>
AVSS	VTD_GR<9>	B5	B11	B17	B23	B29	VTD_GR<11>	B35	B41	B47	B53	B59	VTD_GR<15>	AVSS

Figure 3. Ball location on the chip carrier.

SPECIFICATIONS

Table 2. Absolute maximum electrical ratings

Description	Min	Max	Units
Power supply AVDD	-0.5	1.5	V
Power supply DVDD	-0.5	1.5	
Power supply VDD18	-0.5	2.0	V
Junction temperature	-20	75	ºC
End Of Life (EOL)	10		years

DC Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Electrical Specifications.

Parameter	Min	Typ	Max	Units	Notes
Power Supply					
Power Supply (AVDD)	0.95	1.0	1.05	V	
Power Supply (DVDD)	0.95	1.0	1.05	V	
Power Supply (VDD18)	1.71	1.8	1.89	V	
Power Supply Current (AVDD)		200	300	mA	
Power Supply Current (DVDD)		1.4	1.7	A	
Power Supply Current (VDD18)		5		mA	
Inputs					
Logic control high level	1.62	1.8	1.98	V	
Logic control low level		0.0	0.32	V	
Termination Resistance at the Inputs ARM1<63:0> and ARM2<63:0>	50	50	Hi-Z	Ω	Single ended, measured at DC. Adjustable input termination 50Ω/100Ω/200Ω/Hi-Z for parallel chip connection
Outputs					
Logic high level	1.62	1.8	1.98	V	
Logic low level		0.0	0.32	V	
ESD Protection					
HBM		2		kV	
MM		500		V	
CDM		200		V	

Table 4. AC Electrical Specifications

I/O Port	Parameter	Min.	Typ.	Max.	Units
Clock input **CLOCK**	Frequency		1.0		GHz
	Duty cycle	40	50	60	%
	Signal range	-20			dBm
	Impedance		50		Ω
	Reflection (S11)			-15	dB
	Clock input swing		1 (CMOS)		V
Signal inputs **ARM1, ARM2**	Frequency range	5		500	MHz
	Signal range	-20		-10	dBm
		63		200	mV, p-p
	Impedance	40	50	60	Ω
	Reflection (S11)			-15	dB
	Noise Figure (Input referred)	16.2	17.4	19.4	dB
	Channel-to-channel coupling. Neighboring channels			-30	dB
	Channel-to-channel coupling. Remote channels			-40	dB
Correlation array mode input **XCM_MODE**	Period range		10		ms
	Typical voltage level	0		1.8	V
	Rise/Fall time		200		ps
Output mode input **OUTPUT_ENABLE**	Typical voltage level	0		1.8	V
	Rise/Fall time		200		ps
I^2C interface clock input **SCL**	Clock frequency range	0		0.4	MHz
	Typical voltage level	0		1.8	V
	Rise/Fall time			120	ns
I^2C interface data input **SDA**	Typical voltage level	0		1.8	V
	Rise/Fall time			120	ns
I^2C and ASIC reset input **RST**	Typical voltage level	0		1.8	V
	Rise/Fall time			120	ns
Clock input **CLK_FPGA**	Clock frequency range			250	MHz
	Typical voltage level	0		1.8	V
	Duty cycle	40	50	60	%
	Rise/Fall time		200		ps
Clock output	Clock frequency range		18.496	250	MHz

I/O Port	Parameter	Min.	Typ.	Max.	Units
CLK_DATA	Typical voltage level	0		1.8	V
	Duty cycle	40	50	60	%
	Rise/Fall time		200		ps
Chip state output **XC_READY**	Period range		10		ms
	Typical voltage level	0		1.8	V
	Rise/Fall time		200		ps
Data output **DATA_LINE<7:0>**	Frequency range			125	MHz
	Typical voltage level	0		1.8	V
	Rise/Fall time		200		ps
Test output **TEST_PAD**	Frequency range			10	MHz
	Typical voltage level	0		1.8	V

Table 5. General Specifications

Parameter	Min	Typ	Max	Units	Notes
Number of Channels		64x2			Single ended. AC coupled, provides the on-chip termination for inputs.
Technology for implementation					45nm SOI CMOS
Interface type		I^2C			
ADC bit number		2		bit	Single ended CMOS levels (sign, magnitude)
ADC number of levels		3			
ADC ENOB	1.56			bit	
ADC SFDR	18.5			dB	
ADC SINAD	11.2			dB	
AGC loop response		100		KHz	
VGA gain	28.15	31.68	34.27	dB	
VGA 1dB compression point	-29.6	-27.7	-25.5	dBm	

CONTROL BITs DESCRIPTION

Table 6. I^2C Register Bank Description

Address	Bits	Name	Description	Chg.Set.	Default(hex)	Mode
Configuration bits for local enable and reset						
0	7	vga_adc_en	Analog front end enable		1	R/W
0	6	control_en	Enable input for control unit		1	R/W
0	5	control_rst	Reset input for control unit		0	R/W
0	4	reset_all	Analog front end reset		0	R/W
Configuration bit for transmit data mode						
1	7	read_control	Selecting clock for data transmission 1 – External clock from FPGA 0 – Internally generated clock		0	R/W
Configuration bits for correction						
1	6:4	res_corr[2:0]	Reset offset correction loops 2 – Reset VGA offset compensation 1 - Reset Magn ADC comparators offset compensation 0 - Reset Sign ADC comparator offset compensation		7	R/W
1	3:0	iref_adc_adj[3:0]	Adjust ADC comparators reference current 1111–188uA, 1110–162uA, 1101–140uA, 1100–120uA, 1011–104uA, 1010–88uA, 1001–75uA, 1000–65uA, 0111–56uA, 0110–48uA, 0101–41uA, 0100–35uA, 0011– 30uA, 0010–26uA, 0001–22uA, 0000–19uA		8	R/W
2	7:0	rel[7:0]	Adjustment target ADC LSB duty cycle for VGA AGC system		4B	R/W
3	7:6	range[1:0]	Adjustment of ADC conversion range 00 – 200mV, 01 – 267mV, 10 – 334mV, 11 – 400mV		1	R/W
Configuration bits for transmit data mode						
3	5:0	hlPrdMux [5:0]	Setup half period for MUX clock		1B	R/W
Configuration bits for test mode						
4	1	adc_test_en	Enable test mode for ADC		0	R/W
4	0	adc_test_clkdiv_en	Enable clock divider to reduce the data flow in test mode		0	R/W
Integration time setup						
5	7:0	set_time[7:0]	Setup correlation and integration time		41	R/W
6	7:0	set_time[15:8]	Setup correlation and integration time		54	R/W
7	7:0	set_time[23:16]	Setup correlation and integration time		89	R/W

Table 6. I²C Register Bank Description, continuation

Address	Bits	Name	Description	Chg.Set.	Default(hex)	Mode
Configuration bits for correction						
8	7:4	vtd_vga_adj[3:0]	Adjust VGA input cascade common mode voltage 1111 – 465mV 1110 – 490mV Linear step 26.6mV 0000 – 865mV		A	R/W
8	3:1	iref_vga_adj[2:0]	Adjust VGA reference current (per 8 VGAs) 111 – 325uA 110 – 300uA Linear step 25uA 000 – 150uA		4	R/W
BIAS Configuration bit						
8	0	bias_res_int_ext_sel	Select type of reference current: 0 – from external resistor, 1 – from internal resistor		1	R/W
Configuration bits for test mode						
9	7	do_bist	Start BIST checking 1 – BIST, 0 – other mode		0	R/W
Configuration bits for correction						
0A	7:6	iref_chp_adj[1:0]	Charge-pump output current value adjustment 00 – 0.625uA, 01 – 1.25uA, 10 – 1.875uA, 11 – 2.5uA		0	W
0A	5:4	r_in[1:0]	VGA input termination resistance 00 – 50Ohm, 01 – 100Ohm, 10 – 200Ohm, 11 – Hi-Z state		0	W
0A	3:0	clk_dly<3:0>	Input clock delay adjustment 0000–30ps, 0001–194ps, 0010–214ps, 0011–232ps, 0100–247ps, 0101–263ps, 0110–282ps, 0111–300ps, 1000–321ps, 1001–337ps, 1010–356ps, 1011–375ps, 1100–394ps, 1101–410ps, 1110–429ps, 1111–446ps		0	W
0A	7:0	Status[7:0]	Bitwise BIST result	N	0	R
Status flags						
0B	7:6	Selection[1:0]	Register for selection of BIST bitwise results 00 – 7:0, 01 – 15:8, 10 – 23:16, 11 – 31:24		0	R/W
0B	5	-	Reserved		0	R/W
0B	4	TestOk	BIST checking result 1 – OK 0 – Some bits in result are failing. Pattern can be read using Status[7:0] and Selection[1:0].	N	1	R
0B	4	-	Reserved		0	W

0B	3	-	Reserved		0	W
0B	2:0	cid[2:0]	Chip identification bits	N	0	R
0B	2:0	-	Reserved		0	W

OPERATING MODES

Table 7. Status Table

Nr	Description	Control signals*		
		ENABLE	OUTPUT ENABLE	XCM_MODE
1	ASIC is disabled. DATA_LINE<7:0> and CLK_DATA outputs are in Hi-Z state.	0	0	0
		0	0	1
	ASIC is disabled. DATA_LINE<7:0> and CLK_DATA outputs are in certain logical states.	0	1	0
		0	1	1
2	ASIC is enabled. Reading data mode. DATA_LINE<7:0> and CLK_DATA outputs are in Hi-Z state.	1	0	0
3	ASIC is enabled. Cross-correlation mode. DATA_LINE<7:0> and CLK_DATA outputs are in Hi-Z state.	1	0	1
4	ASIC is enabled. Reading data mode. DATA_LINE<7:0> and CLK_DATA outputs are in certain logical states.	1	1	0
5	ASIC is enabled. Cross-correlation mode. DATA_LINE<7:0> and CLK_DATA outputs are in certain logical states.	1	1	1

Note: *"0" – Low logical level, "1" – High logical level.

THE BASIC MODE OF OPERATION ASIC

INITIALIZATION

During the power supplies rump-up, the POR circuit generates internal reset impulse for internal digital blocks. This internal reset impulse initializes digital core such as I^2C interface, control block, cross-correlation matrix and calibration circuit in the AGC. After turning on the ASIC by signal ENABLE, 200ms is required for the analog front-end initialization (Figure 4). Afterwards, the chip is ready for the correlation process.

CROSS-CORRELATION

The ASIC enters into the cross-correlation mode by a signal input XCM_MODE from a LOW logic state to a HIGH logic state, (Figure 4). In this mode, it performs cross-correlation between the analog signals from the inputs ARM1[63..0] and ARM2[63..0]. The cross-correlation time is determined by the internal programmable register or by an input control signal XCM_MODE. The end of the cross-correlation mode is indicated by the external signal XC_READY. Changing in the state of XCM_MODE signal switches the ASIC to the data transmission mode (READING DATA).

DATA READOUT

The ASIC switched to the data reading mode by a signal at the XCM_MODE input switched from a HIGH logic state to a LOW logic state (Figure 4). Data is transmitted via the data bus DATA_LINE[7..0]. CLK_DATA signal is used as a synchronization signal for the data transmission.

STANDBY

In the standby mode, the ASIC is waiting for the changes of control signals.

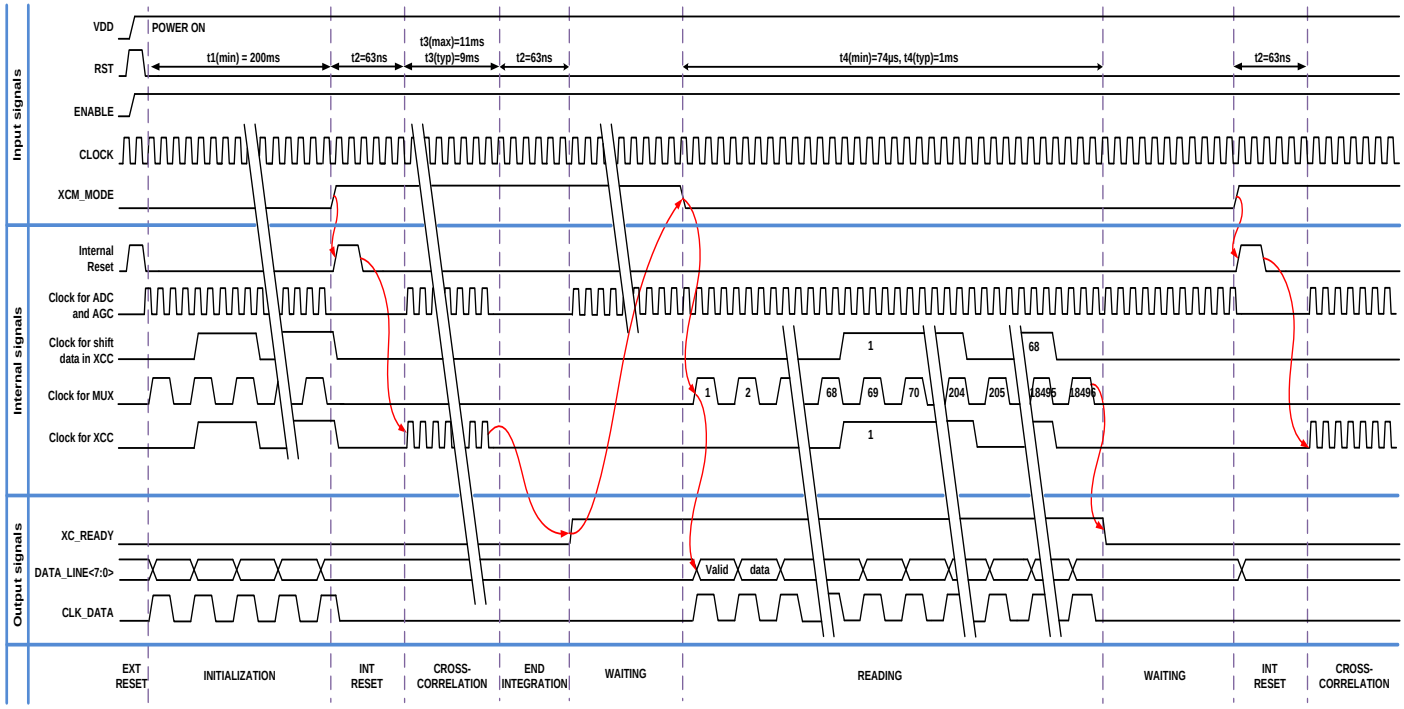


Figure 4. Timing diagram.

OPERATING PROCEDURE FOR THE ASIC

ENABLE

1. set power supply VDD18, AVDD and DVDD
2. apply to CLOCK input clock signal 1GHz
3. set OUTPUT_ENABLE input to "0"
4. set ENABLE input to "1"
5. set XCM_MODE input to "0"
6. wait 200ms for the analog front-end initialization

CROSS-CORRELATION

1. set XCM_MODE input to "1"
2. when XC_READY set to "1", correlation is finished

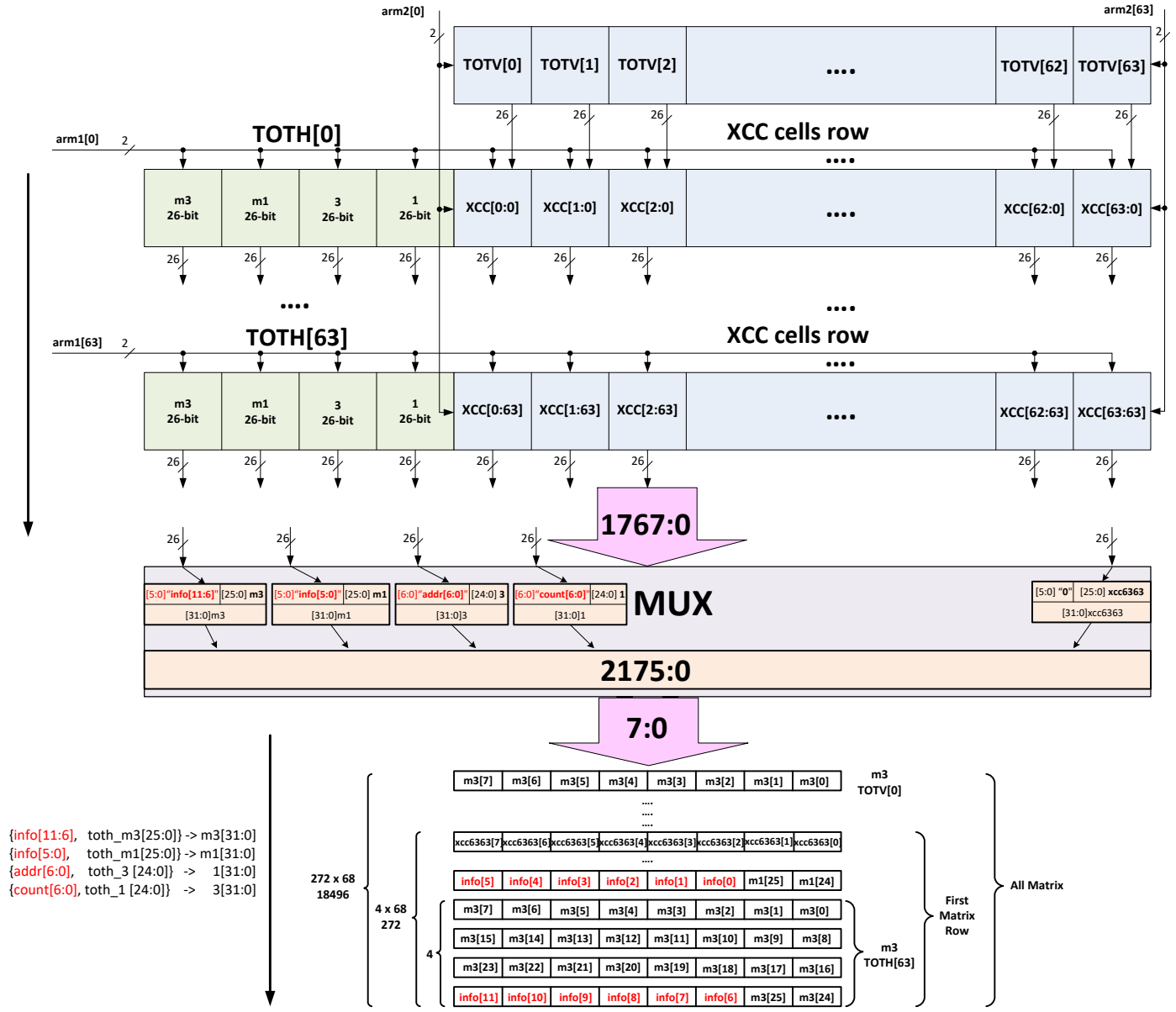
READING DATA

1. set XCM_MODE input to "0"
2. set OUTPUT_ENABLE input to "1"
3. read data from DATA_LINE<7:0>
4. when XC_READY set to "0", data transmission is finished
5. set OUTPUT_ENABLE input to "0"

DISABLE

1. set ENABLE input to "0"

OUTPUT DATA PACKET STRUCTURE



Red Color – Service Information (ASIC ID, number of line, other info)

Readout sequence:

1. 26-bit data output in every cell from matrix row (XCC or TOT*) complements to 32 bits by adding “0” values as MSB.
2. MUX has 8-bit output, it means data from every cell will contain 4 packets of 8 bits started from six “0s” in the first packet.
3. The first four packets contain TOTH[63] m3 value, then m1, 3,1, XCC[63:63], …, XCC[0:63]. There is a total of 272 packets from one row.
4. The last four packets contain TOTV[0] m3 value.

Size of the single frame readout from the cross-correlator is 18496 bytes.

ASIC APPLICATION NOTES

The following recommendations should be taken into account during the integration of the ASIC on the PCB.

The multiple ASIC connection to a common readout bus:
The SAR Rx signal processing ASIC has adjustable VGA input termination 50Ω/100Ω/200Ω/Hi-Z for parallel connection of DATA_LINE outputs to a common readout bus.

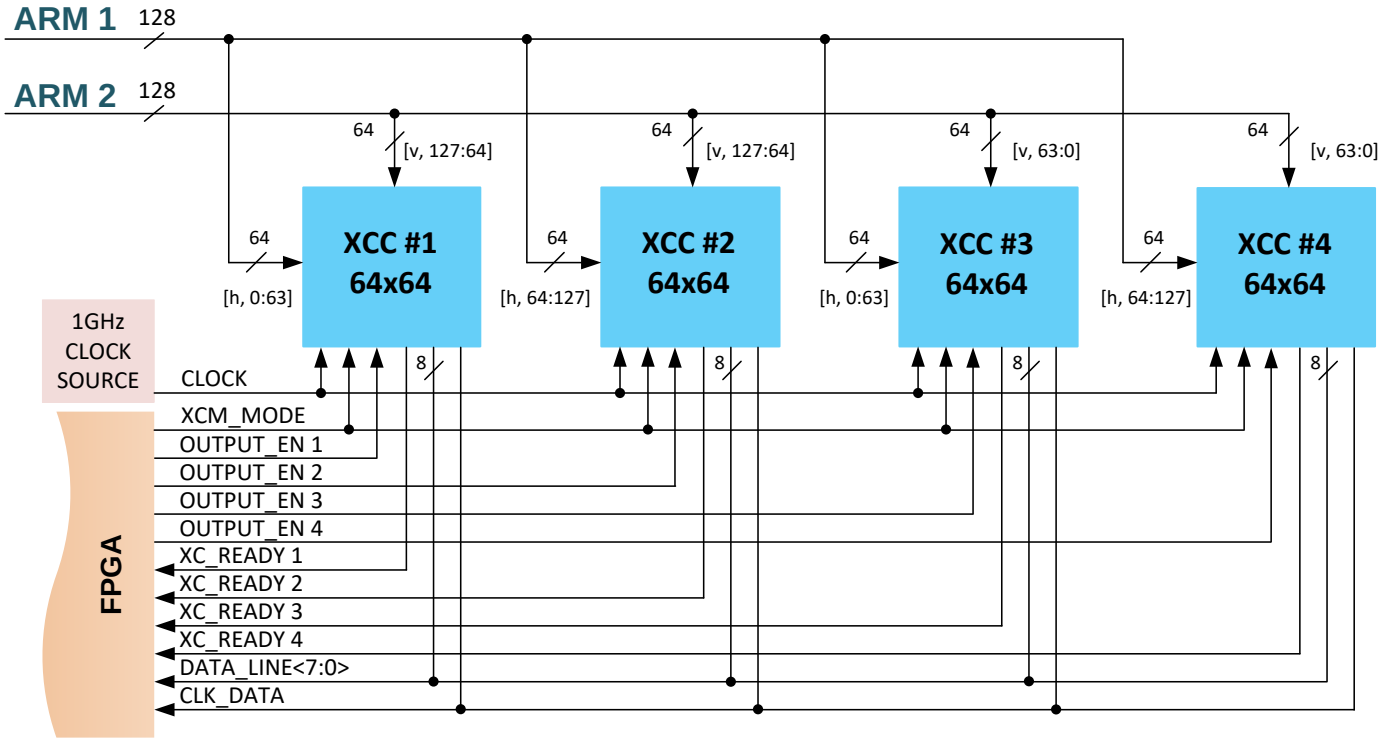


Figure 3. Connection of four ASICs to a common readout bus.

Input signals interconnects:

1. Keep all analog ARM1<63:0> and ARM2<63:0> signals routing as small as possible and maintain the same interconnect length.
2. Signals to ARM1 and ARM2 should be supplied through external 100nF DC blocking capacitors.
3. Ensure good quality low jitter clock according to system specifications.
4. Rise and fall time of control signals must not exceed recommended values.

Output bus:

1. The maximum value of the output load capacitance for nets DATA_LINE<7:0>, CLK_DATA and XC_READY is 20pF.
2. Keep the minimum length and resistance of interconnects between RES_EXT_PAD and resistor on PCB.