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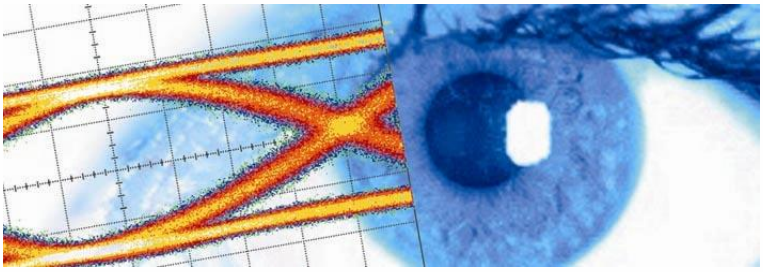


Datasheet
SHF 19120 C

2.85 GSa/s Arbitrary Waveform Generator with 4x 10.3 Gbps BPG Outputs

For illustration only, actual product may vary

Description

The SHF 19120 C is a 2.85 GSa/s, 14 bit Arbitrary Waveform Generator (AWG) with four 10.3125 Gbps bit pattern outputs. Its high AWG bandwidth (>1.4 GHz), high output amplitude (1.2 V on DC output, +10 dBm on the AC output) and large sample memory size (1 Giga Sample) make it a versatile arbitrary generator.

Three outputs (Direct, DC and AC) cover a wide range of test scenarios (jitter, glitched signal, modulation and modulated signal generation, etc.)

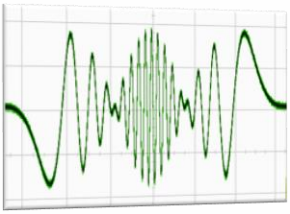
Two markers with a 2-sample resolution can be used to trigger external equipment. Two edge/level trigger inputs with adjustable thresholds start, pause or restart the signal generation.

Two or more SHF 19120 C instruments can be synchronized together via their 10 MHz references.

A sample sequencer allows the creation of complex waveforms with memory-saving repeated patterns (to be enabled in the future with a software update).

In addition to the three analog outputs, the SHF 19120 C can generate up to four 10.3125 Gbps PRBS signals with emphasis on the rear panel, driven by the DAC clock, or by an external clock.

The SHF Control Center software allows a complete control of the SHF 19120 C, including a waveform editor with a waveform library and a Python equation editor. When connecting a keyboard, a mouse and a monitor, the SHF 19120 C can be controlled without a computer, via the embedded version of the SHF Control Center.



SHF 19120 C: actual waveform and GUI

Features

- Arbitrary Waveform Generator
  - Sampling frequency f_{DAC} up to 2.85 GHz
  - 1 GSa – sample memory
  - Three types of outputs: Direct, DC coupled (1.2 V_{pp}) and AC coupled (+10 dBm max, in 0.1 dB steps)
  - High output bandwidth: DC to 1.4 GHz for the direct and DC outputs, 20 MHz to 500 MHz for the AC output
  - Up-sampling: in the Double Interpolation Mode, the signal spectrum is shifted to f_{DAC}, doubling the effective DAC update rate
  - Two sample-synchronous marker outputs
  - Two trigger (edge/level) inputs with adjustable thresholds
  - Output skew control in combination with trigger and marker delays help the synchronization of several SHF 19120 C AWGs
  - Outputs and inputs for the DAC and BPG clock, and the 10 MHz reference
- Bit Pattern Generator
  - Four PRBS differential outputs with lane bitrates from 0.372 Gbps to 10.3125 Gbps with the possibility of overclocking to 12.5 Gbps
  - Nine PRBS patterns (from $PRBS^{7}$-1 to $PRBS^{31}$-1), plus two square wave patterns of half line rate (SQUARE2) and line rate ÷ 32 (SQUARE32) and user-defined patterns (4 Gb per channel)
  - Frame trigger output
  - Bit skew adjustment
  - Pre and post cursor emphasis
- Computer controlled via a 1 G Ethernet link or
- Stand-alone operation, with keyboard, mouse and monitor
- Modern and user-friendly software

Applications

- Jitter modulation source
  - random noise with a Crest factor up to 17 dB
  - Sinusoidal
  - PRBS
  - Multi-frequency and multi-tone
  - Custom shapes

- Telecommunication
  - Generation of real-world waveforms
  - Utrawide band signals
  - Development of long-haul data transmission schemes
  - Compliance testing
  - Step response and bandwidth measurements
  - Wireless communications
  - Backplane characterization
  - High speed serial link testing
  - Clock source

- Optics
  - Shaped pulses
  - Photonics research

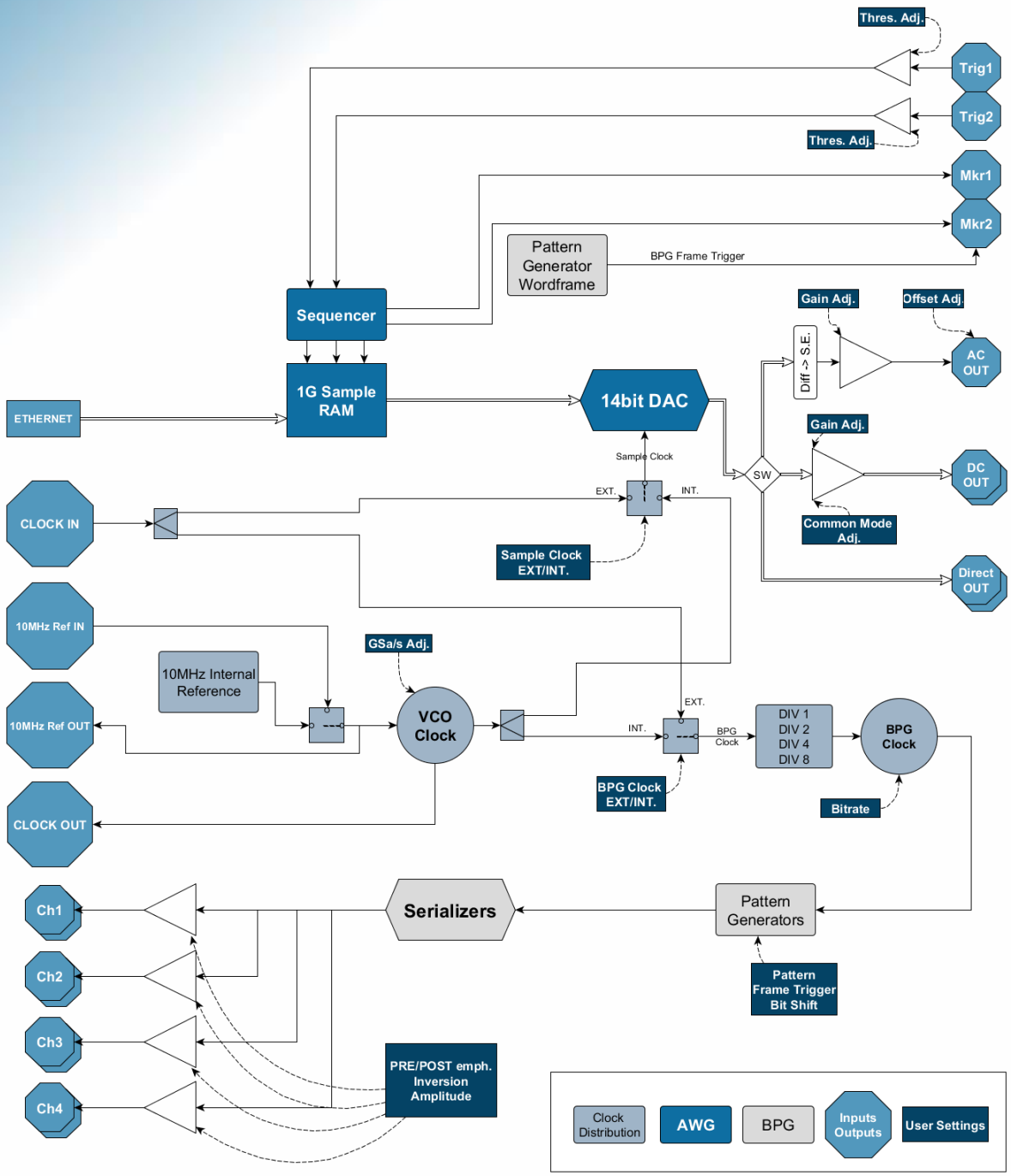
- Medicine
  - Simulating complex ECG patterns
  - Living cell stimulation

- Radar / Lidar
  - Chirp generation
  - Shaped signal generation

- Physics
  - Reflectometry
  - Nuclear magnetic resonance research
  - Study of materials
  - Mass spectrometry experiments

- Quantum Computing and quantum measurements
- Development of Test and Measure Equipment
- Radar signals
- Multilevel signals

Block Diagram



Absolute Maximal Ratings

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Power Supply Voltage	V				13	
Trigger Inputs	V		0		5	CMOS, DC coupled
Clock Input	dBm				3	AC coupled
10 MHz Input	V				3.3	Peak-to-Peak, AC coupled

Specifications – SHF 19120 C

Unless specified, all measurements are taken single-ended, with f_{DAC} = 2.85 GHz.

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Power Supply Voltage	V		11.6	12	12.4	+12V switching power supply is included
Power Supply Current	A		2	2.5	3	
Power Consumption	W			30		
Operating Temperature	°C		10		35	
General characteristics - AWG						
Resolution	bits			14		Markers do not decrease the resolution or memory size.
Sample Rate	GSa/s	f_{DAC}	1.4		2.85	
RF Connectors				SMA		
Output Adjustable Delay	Sample Clock Periods		0		254	
Output Adjustable Delay Step	Sample Clock periods		2			
General characteristics - BPG						
Channels				4		
Bit Rate	Gbps		0.372		10.3125	Overclocking up to 12.5 Gbps possible. See bit rate ranges, page 12
RF Connectors				SMA		Differential
External Clock Input Multiplier Factor			1		8	The BPG bitrate will be the external clock frequency multiplied by this factor
Adjustable Delay Length	bit		-Pattern Length		+Pattern Length	With a 1 bit step

Direct Output						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Impedance	Ohm			50		
Voltage Window Minimum	mV		205		215	Single-ended. Includes the output offset from internal biasing
Voltage Window Maximum	mV		750		760	Single-ended. Includes the output offset from internal biasing
Adjustable Full-Scale Amplitude Minimum	mV			210		Single-ended, Peak-to-Peak
Adjustable Full-Scale Amplitude Maximum	mV			760		Single-ended, Peak-to-Peak
Full-Scale Amplitude Step	mV			5		
Full-Scale Amplitude Accuracy				±(50mV ±10%)		
Random Jitter RMS	ps	J_{RMS}		4		Measured with PRBS-7, sample clock for trigger.
Rise/Fall Time	ps	t_r/t_f		110		0.7V, 1.425 GHz square signal, from 20% to 80%
3dB Bandwidth	MHz		1400			Not compensated for the sinx/x DAC response.
Calculated Bandwidth	MHz			2000		$\frac{0.223}{tr}$
SFDR *Spurious Free Dynamic Range*	dBc			-81		32 Samples sine wave (89.0625 MHz), 0.63 Vpp signal. Harmonics excluded, 40 dB interpolation filter enabled.
Two-Tone IMD *Inter Modulation Distortion*	dBc			-56		f_1= 19.9 MHz f_2= 20.1 MHz ; 630 mV_{pp} ; $2f_2-f_1$
Harmonic Distortion	%			0.7		101.7857 MHz Output, 630 mV_{pp} ; 5 first harmonics.

Direct output: Differential or Single-ended output (Unused output must be terminated with a 50 Ω load), DC-coupled.

All the SHF 19120 C AWG outputs are unfiltered, to give the user the most versatile bandwidth. Depending on the application, an external low or high pass filter is recommended.

DC Output						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Impedance	Ohm			50		
Voltage Window Minimum	mV				-200	The signal will be clipped outside the voltage window
Voltage Window Maximum	mV		1200			The signal will be clipped outside the voltage window
Adjustable Full-Scale Amplitude Minimum	mV			360		Single-ended, Peak-to-Peak
Adjustable Full-Scale Amplitude Maximum	mV			1300		Single-ended, Peak-to-Peak
Full-Scale Amplitude Step	mV			5		
Full-Scale Amplitude Accuracy				±(50mV ±10%)		
Adjustable Offset	mV		150		650	Limited by the output voltage window
Offset Step	mV			1		
Offset Accuracy	mV			±50		
Random Jitter RMS	ps	J_{RMS}		6		Measured with PRBS-7, 0.7 V_{pp}, sample clock for trigger.
Rise/Fall Time	ps	t_r/t_f		120		Measured with PRBS-7, 1 V_{pp}, sample clock for trigger, from 20% to 80%
3dB Bandwidth (from DC)	MHz		1400			Not compensated for the sinx/x DAC response.
Calculated Bandwidth	MHz			1850		$\frac{0.223}{tr}$
Bandwidth Ripple (0 – 1400 MHz)	dB			1		
SFDR *Spurious Free Dynamic Range*	dBc			-71		32 Samples sine wave (89.0625 MHz); 1 Vpp with 0.6 V offset signal ; harmonics and f_{DAC} excluded, 40 dB interpolation filter enabled.
Two-Tone IMD *Inter Modulation Distortion*	dBc			-56		f_1= 19.9 MHz f_2= 20.1 MHz ; 700 mV_{pp} ; $2f_2$-f_1
Harmonic Distortion	%			0.2		101.7857 MHz Output, 630 mV_{pp} ; 5 first harmonics.

DC output: Differential or Single-ended output (Unused output must be terminated with a 50 Ω load), DC-coupled

All the SHF 19120 C AWG outputs are unfiltered, to give the user the most versatile bandwidth. Depending on the application, an external low or high pass filter is recommended.

AC Output						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Impedance	Ohm			50		
Adjustable Full Scale Amplitude Minimum	dBm				-27	
Adjustable Full Scale Amplitude Maximum	dBm		10		14	
Adjustable Amplitude Step	dB			0.1		
Accuracy	dBm			0.2	0.4	
Adjustable Bias	V		0		4.5	Integrated bias tee
Adjustable Bias Step	mV			10		
Offset Accuracy	mV			±50	±100	
Bias Output Current	mA				150	
3dB Bandwidth (starting at 20 MHz)	MHz		500			Not compensated for the sinx/x DAC response.
6dB Bandwidth (starting at 20 MHz)	MHz		1400			Not compensated for the sinx/x DAC response.
SFDR *Spurious Free Dynamic Range*	dBc			-71		32 Samples sine wave (89.0625 MHz) 0 dB Output, harmonics and f_{DAC} excluded, 40 dB interpolation filter enabled. DC to $f_{DAC.}$
Two-Tone IMD *Inter Modulation Distortion*	dBc			-55		f_1= 99.45 MHz f_2= 100.45 MHz ; 0 dBm output; f_{DAC}= 2.12 GHz ; $2f_2$-f_1
Harmonic distortion	%			0.3		101.7857 MHz Output, 0 dBm output 5 first harmonics.
Double Interpolation mode						
SFDR *Spurious Free Dynamic Range*	dBc			-55		30-Sample sine wave, -10 dBm Output, harmonics excluded DC to $f_{DAC.}$
Two-Tone IMD *Inter Modulation Distortion*	dBc			-63		f_1= 2.28001 GHz f_2= 2.2857 GHz ; 0 dBm output; f_{DAC}= 2.85 GHz ; $2f_2$-f_1

AC output: Single-ended output, AC coupled, with adjustable offset.

All the SHF 19120 C AWG outputs are unfiltered, to give the user the most versatile bandwidth. Depending on the application, an external low or high pass filter is recommended.

Markers – Two marker outputs – Front panel						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Amplitude	V		2.1	2.5	2.5	LVCMOS25, DC coupled
Impedance	Ohm			50		Match to 50 Ohms for best signal.
Resolution	Sample			2*		Sample synchronous.
Width	Sample		1		1G	A single marker will be automatically extended to a width of 1ns by the SHF Control Center.
Maximum Repeatability	Sa			3		Each marker must have a dead time of 3 samples before the next marker.
Maximum Frequency	MHz			700		With f_{DAC} =2.85 GSa/s.
Jitter peak-peak	ps			100		Direct output, 32-sample Dirac signal for trigger. 3-sample marker, output 1.
Adjustable Delay	Sample Clock periods		0		254	
Adjustable Delay Step	Sample Clock periods			2		

**2 samples position uncertainty when generating a repeating signal with an odd sample count period and a marker on each period. The SHF Control Center will issue a warning when this situation happens.*

Triggers – Two trigger inputs – Front panel						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Type	Rising edge, falling edge, gated high, gated low.					
Adjustable Threshold Low	V	V_{IL}		1.2		Measured on a 50Ω system.
Adjustable Threshold High	V	V_{IH}		4		Measured on a 50Ω system.
Adjustable Threshold Step	mV			100		Measured on a 50Ω system.
Adjustable Threshold Accuracy	mV			100		Measured on a 50Ω system.
Delay	ns			250 + 200*Sa		From Trigger in to Signal present on output. X ns + Y*Sample Period
Pulse Width	ns		250			
Pulse Frequency in Start/Pause Mode	MHz				2	
Dwell time in Restart Mode	us		4		5	
Trigger Jitter peak-peak	ns			15+10*Sa		X ns + Y*Sample Period
Adjustable Delay	Sample Clock periods		0		510	
Adjustable Delay Step	Sample Clock periods			2		

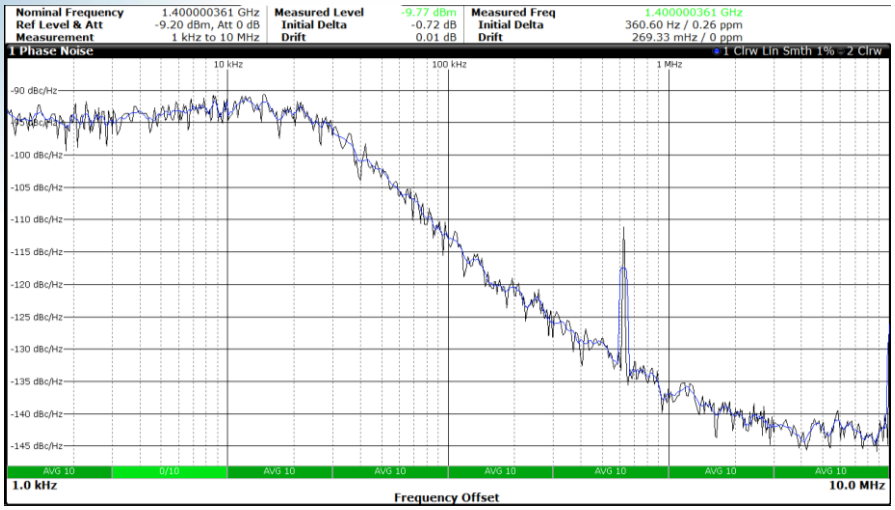
Internal reference						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Frequency	MHz			10		
Accuracy	ppm		-1		1	Over the operational range.
Stability	ppb			280		Over the operational range.
Output Level	V			1		External, back panel.
Output Impedance	Ohms			50		

External reference input						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Frequency	MHz			10		
Level	V		0.5		3.3	Peak-to-Peak.
Impedance	Ohms			50		

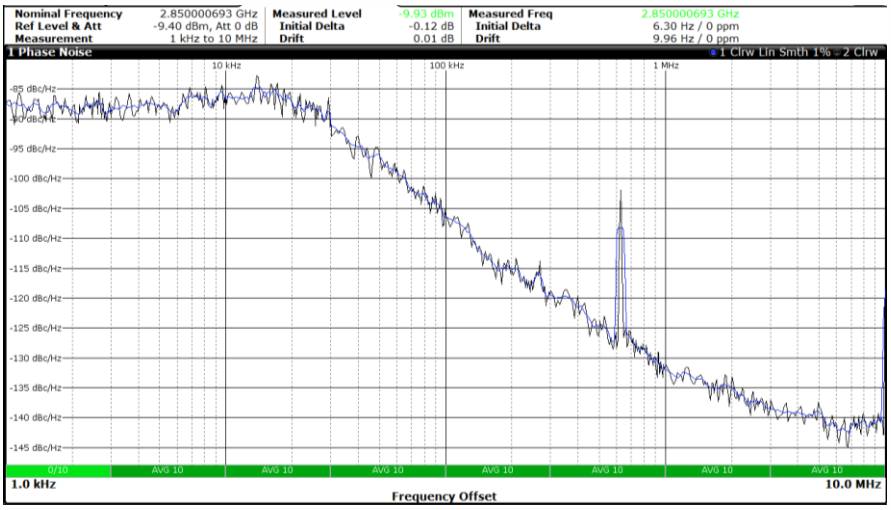
Sample clock						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Frequency	GHz		1.4		2.85	
Output Level	dBm			0		Rear panel, Peak-to-Peak.
Output Impedance	Ohms			50		

Sample sequencer						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Sample Granularity	Sample		1024		1G	
Sample Length			1024		1G	
Segments			1			
Loops			1			
Sample Memory	GSa				1	1 Sample = 14 bits + 2 Markers.

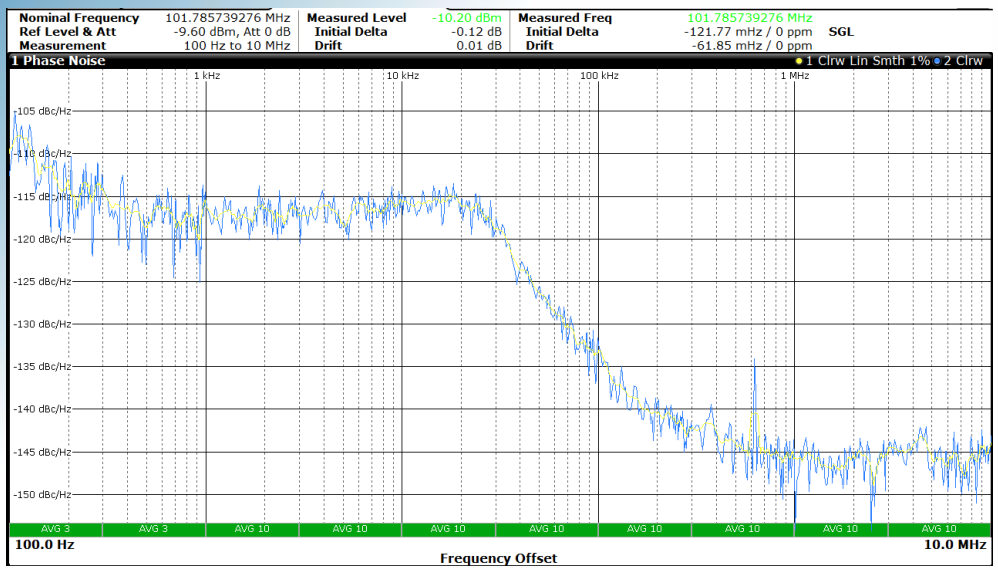
Plots of the phase noise



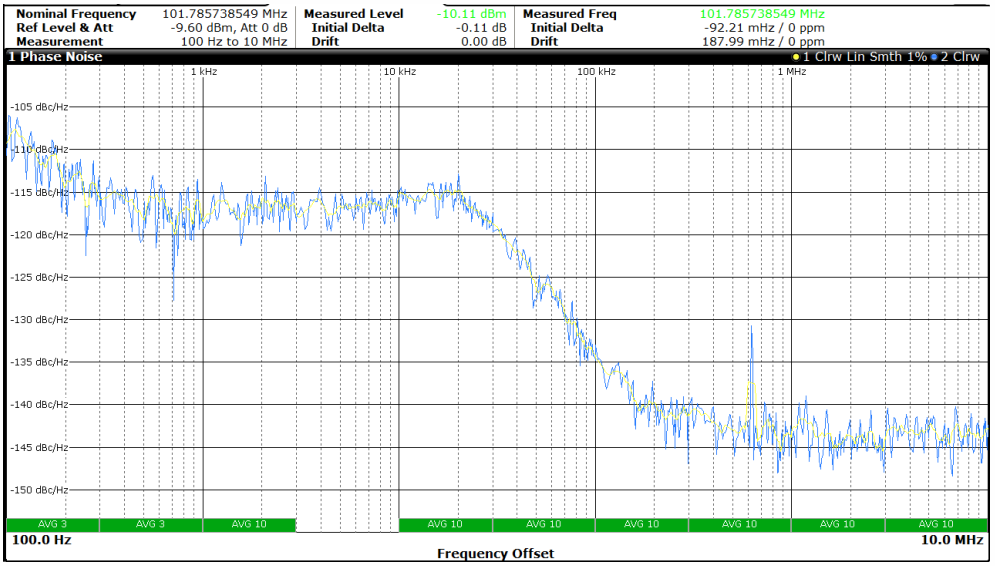
DAC Clock SMA Output, f_{DAC}=1.4 GHz, 10 dB attenuator.



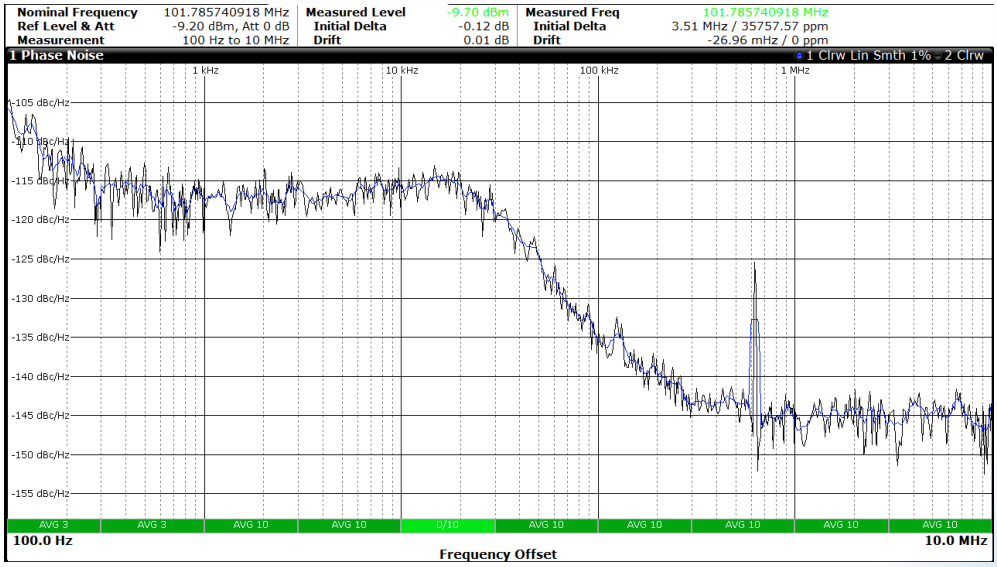
DAC Clock SMA Output, f_{DAC}=2.85 GHz, 10 dB attenuator.



Direct non inverting output. 28–sample sine wave (101.79 MHz), 0 dB output, 10 dB attenuator.



DC non inverting output. 28–sample sine wave (101.79 MHz), 0 dB output, 10 dB attenuator.



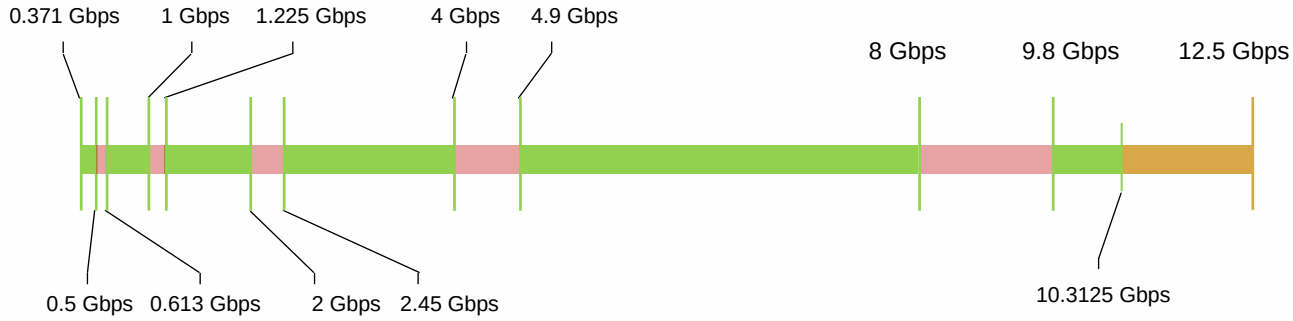
AC output. 28–sample sine wave (101.79 MHz), 0 dB output, 10 dB attenuator.

Bit Pattern Generator Outputs						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Impedance	Ω			50		AC coupled
Output Level Minimum	mV		270			Single Ended, Peak-to-Peak, at 5 Gbps
Output Level Maximum	mV		600	650	700	Single Ended, Peak-to-Peak, at 5 Gbps
Output Level Steps				15		
Pre-emphasis: Precursor	dB		0		6.02	20 steps
Pre-emphasis: Postcursor	dB		0		12.96	31 steps
Jitter RMS	ps			3		At 10.3125Gbps, PRBS31, SQUARE32 for trigger.
Rise/Fall Time	ps			55		At 10.3125 Gbps, PRBS31, SQUARE32 for trigger, from 20% to 80%.
Crossing	%		45	50	55	At 10.3125 Gbps.
Duty Cycle	%			50		At 10.3125 Gbps.
Inter-Channel Skew	ps			40		At 10.3125 Gbps.
Output pattern	ITU-T (CCITT) conform PRBS patterns at a length of: 2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{13}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1, 2^{31}-1 Additional SQUARE2 and SQUARE32 0-1 patterns: line rate divided by 2 and 32. 4 Gb of user pattern per channel.					
Bit Rate (Range 1)	Gbps		0.372		0.5	The bit rate setting is common for all the BPG outputs.
Bit Rate (Range 2)	Gbps		0.613		1	
Bit Rate (Range 3)	Gbps		1.225		2	
Bit Rate (Range 4)	Gbps		2.45		4	
Bit Rate (Range 5)	Gbps		4.9		8	
Bit Rate (Range 6)	Gbps		9.8		10.3125	Overclock up to 12.5 Gbps possible.
Bitrate resolution	Kbps			100		
Wordframe Trigger Division			32		2^{31}-1	Of internal clock cycles. 32 means 32 x (pattern length). Uses the AWG Marker output.
Wordframe Trigger Level	V		2.1	2.5		LVCMOS25, DC coupled
Wordframe Jitter	ps			500		Peak-to-Peak
PRBS Ext. Clock Input Level	dBm		-5		10	50 Ω, AC coupled
PRBS Ext. Clock Input Frequency	MHz		60		2800	Using the internal multiplier

BPG User Pattern*						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Granularity	bits		64			Per channel. The channels must have the same pattern length.
Length			64		4G	Per channel. The channels must have the same pattern length.
Segments			1			
Loops			1			
Memory	Gb				4	Per channel

**Enabling the BPG user pattern disables the AWG function.*

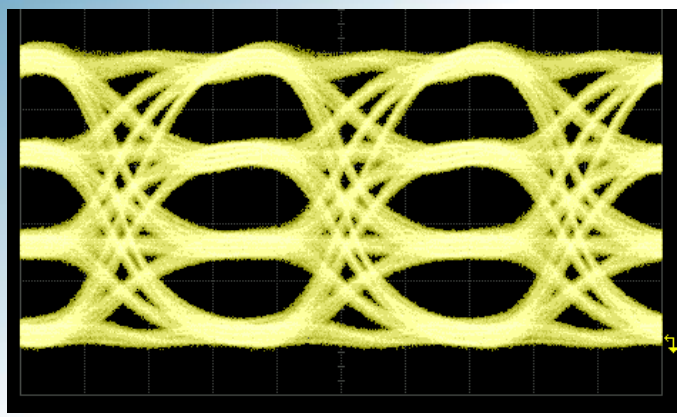
Ranges for the Bit Rate



Pattern Types for the Pseudo Random Binary Sequence

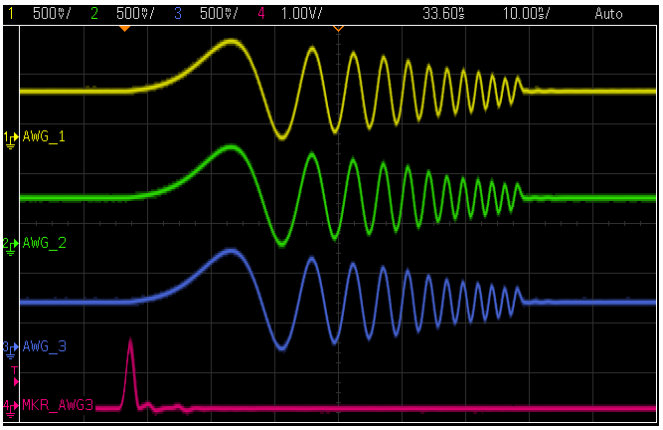
Name	Polynomial	Length
$PRBS2^{7}$-1	$1 + X^{6} + X^{7}$	2^{7} - 1 bits
$PRBS2^{9}$-1	$1 + X^{9} + X^{5}$	2^{9} - 1 bits
$PRBS2^{10}$-1	$1 + X^{10} + X^{7}$	2^{10} - 1 bits
$PRBS2^{11}$-1	$1 + X^{11} + X^{9}$	2^{11} - 1 bits
$PRBS2^{13}$-1	$1 + X^{2} + X^{12} + X^{13}$	2^{13} - 1 bits
$PRBS2^{15}$-1	$1 + X^{14} + X^{15}$	2^{15} - 1 bits
$PRBS2^{20}$-1	$1 + X^{17} + X^{20}$	2^{20} - 1 bits
$PRBS2^{23}$-1	$1 + X^{18} + X^{23}$	2^{23} - 1 bits
$PRBS2^{31}$-1	$1 + X^{28} + X^{31}$	2^{31} - 1 bits

Typical Output Waveforms (AWG)

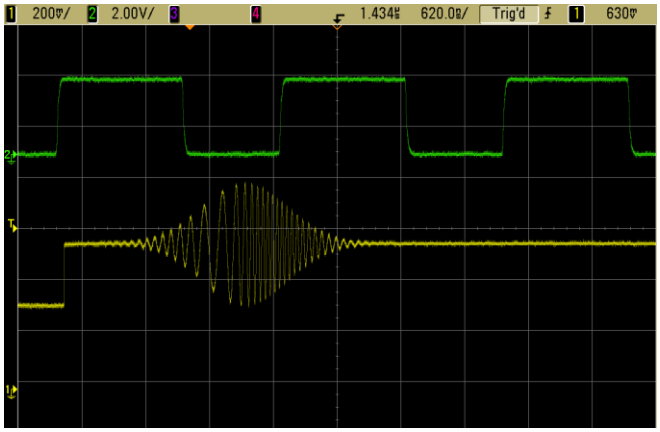


2.85 GSa/s PAM-4 signal, DC Output

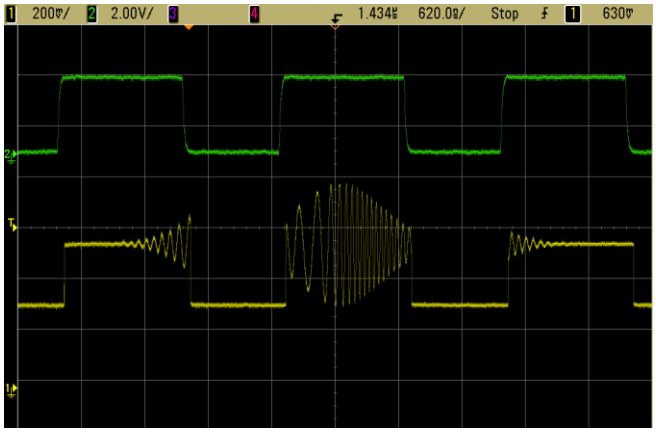
(200 mV/div ; 100 ps/div)



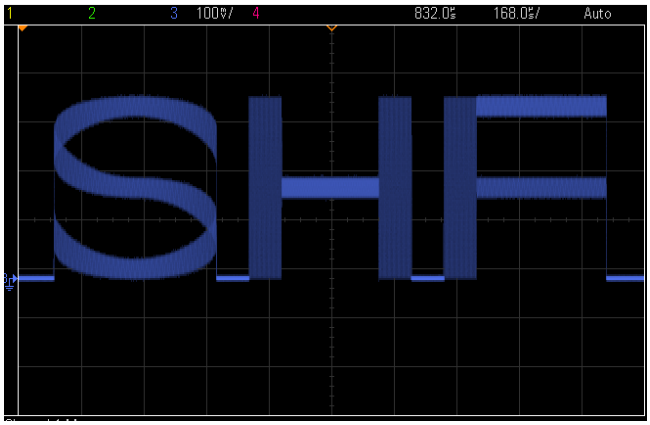
Frequency and phase synchronization of three SHF 19120 C



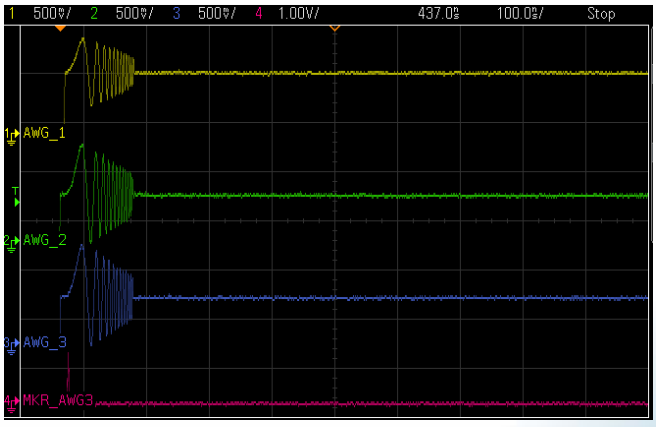
Edge-triggered signal generation.



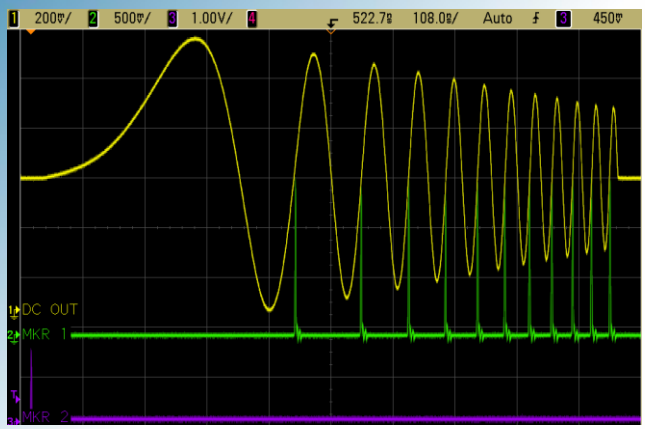
Level-gated trigger signal generation.



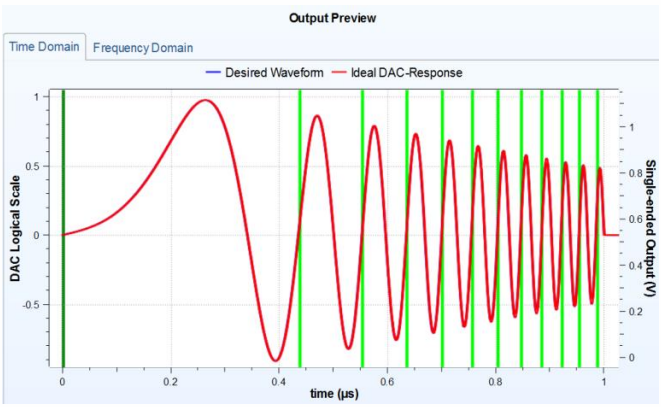
“SHF” writing



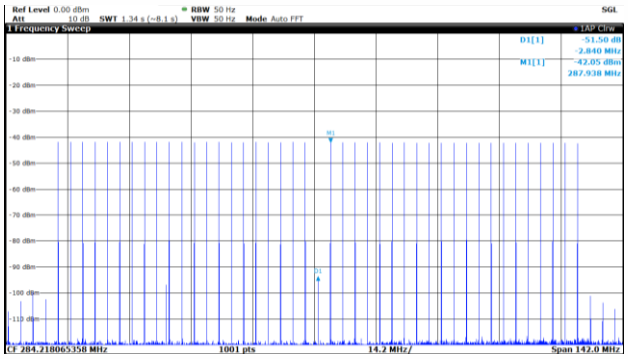
Burst mode of three synchronized SHF 19120 C



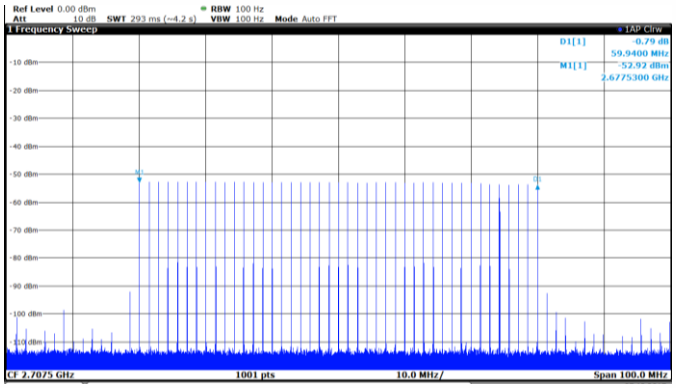
Signal with markers: marker output 1 for each rising part of signal, marker output 2 for the signal start.



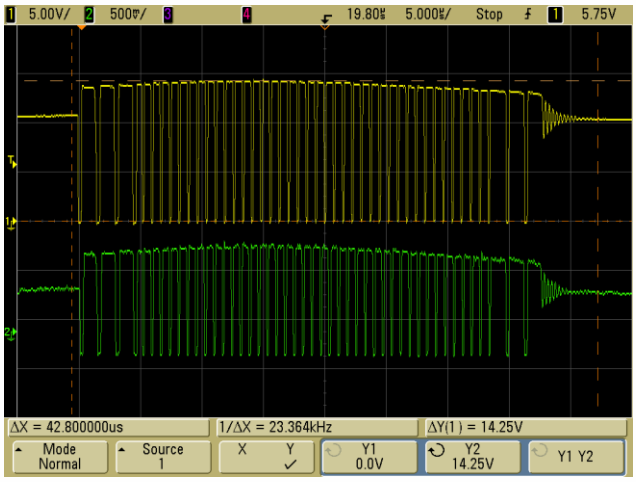
Screenshot from the SHF Control Center preview of the signal shown on the left.



Multiple-Carrier Signal Noise-Power Ratio, AC Output, 0 dBm, 10 dB ext. att.

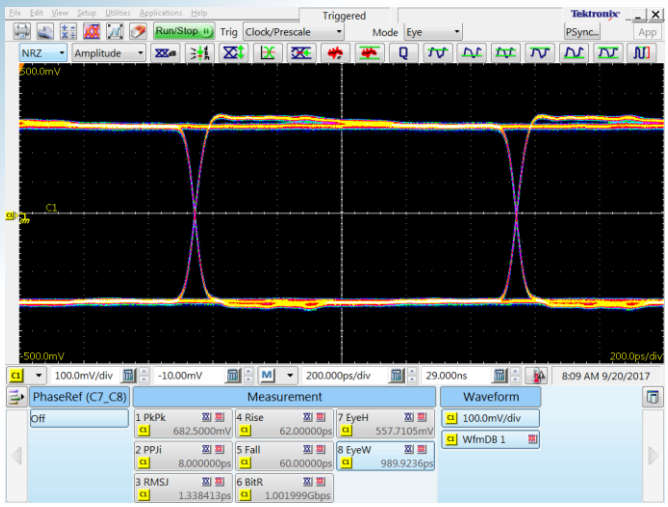


Multiple Carriers in Double Interpolation Mode, AC Output, 0 dBm, 10 dB ext. att.

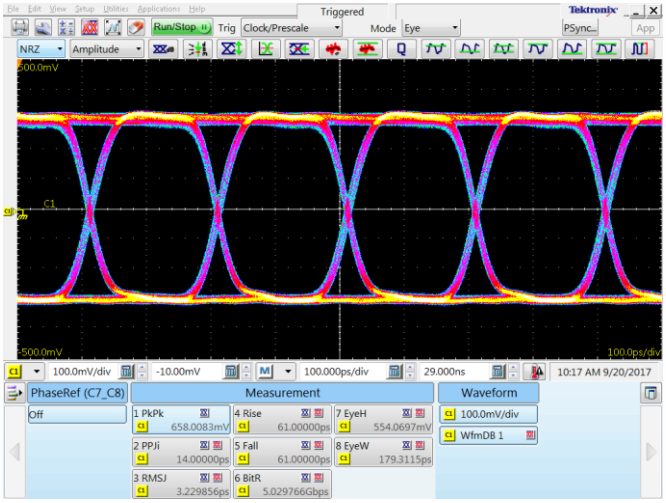


Original (yellow) and AWG waveform (green) after import. Inductor voltage of a Ćuk converter.

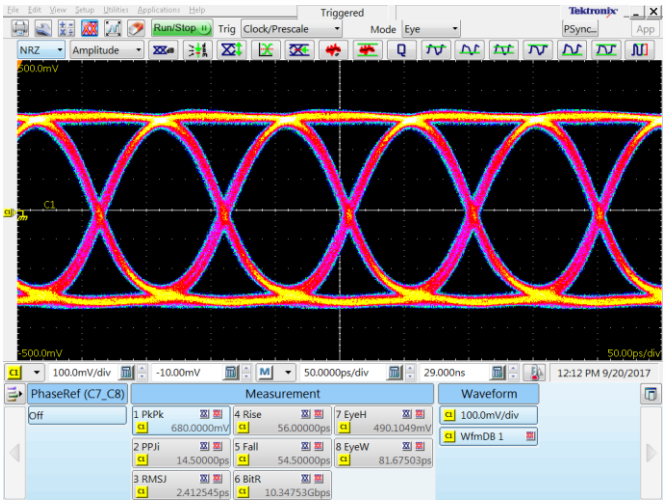
Typical Output Waveforms (BPG)



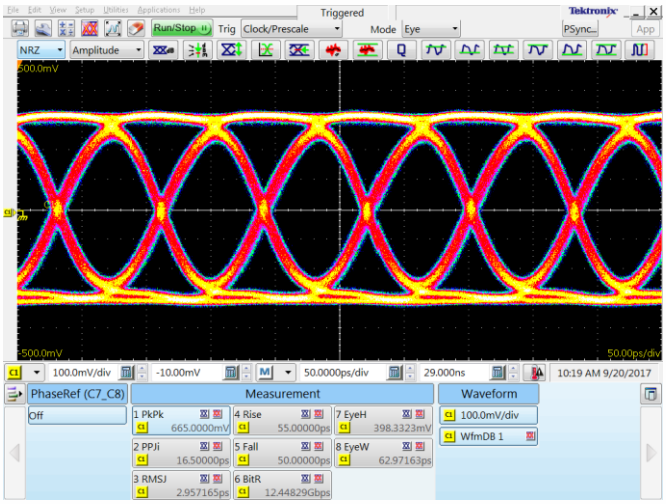
1 Gbps PRBS 2^{31}-1



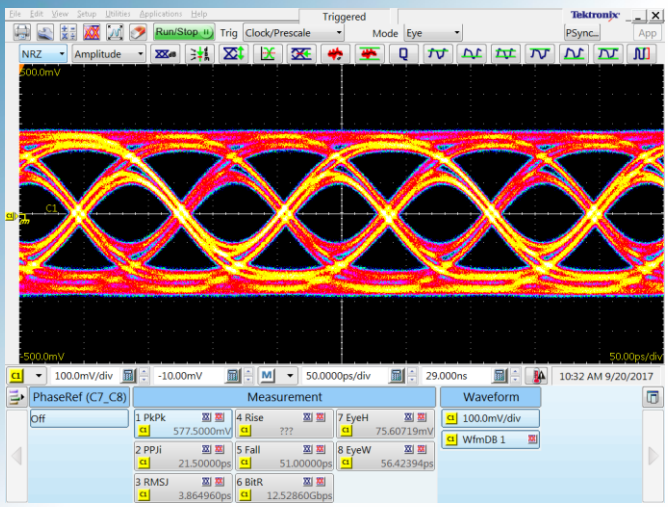
5 Gbps PRBS 2^{31}-1



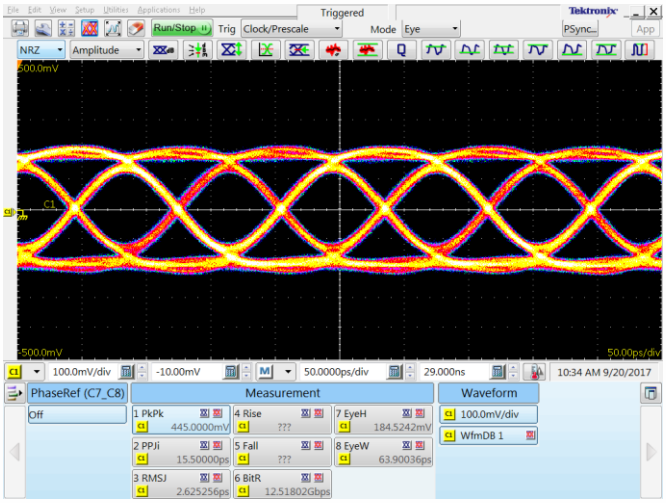
10.3125 Gbps PRBS 2^{31}-1



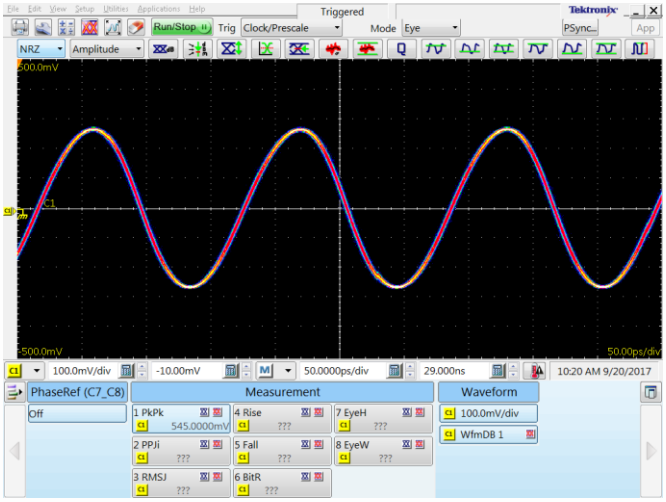
12.5 Gbps PRBS 2^{31}-1



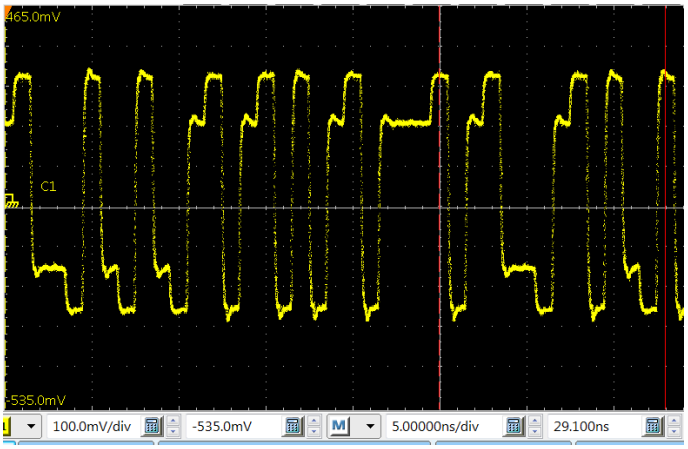
12.5 Gbps PRBS 2^{31}-1 with a 3 meter cable
POST cursor = 0dB PRE cursor = 0dB



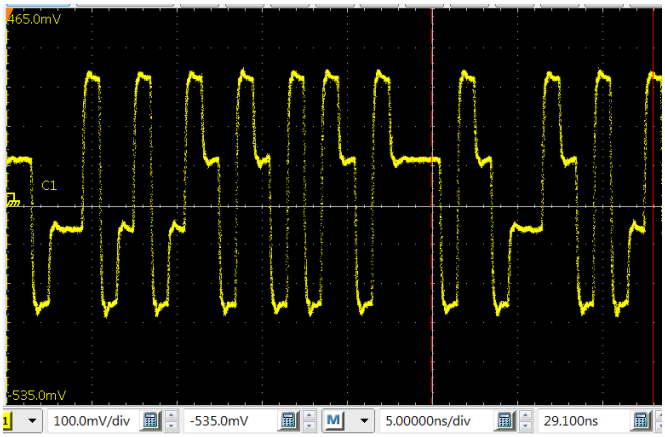
12.5 Gbps PRBS 2^{31}-1 with a 3 meter cable and emphasis enabled
POST cursor = 1.94 dB PRE cursor = 2.5 dB



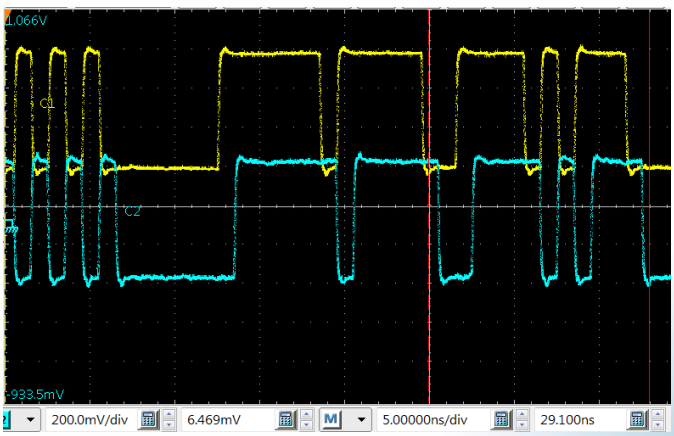
12.5 Gbps SQUARE 2 pattern



Pre-emphasis: precursor – max. value (1 Gbps, PRBS 2^7-1)



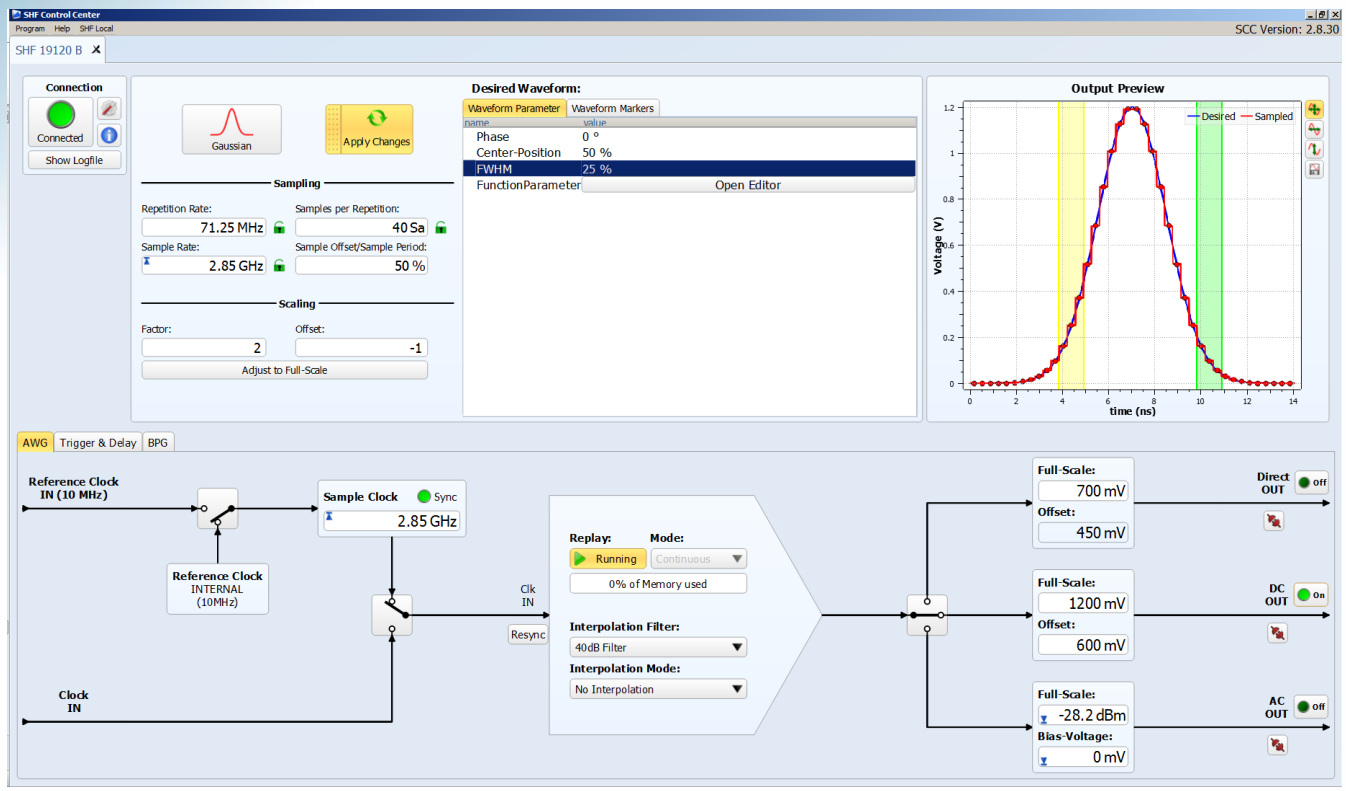
Pre-emphasis: postcursor – max. value (1 Gbps, PRBS 2^7-1)



1 bit pattern shift (1 Gbps, PRBS 2^7-1 ; ch1 and ch2)

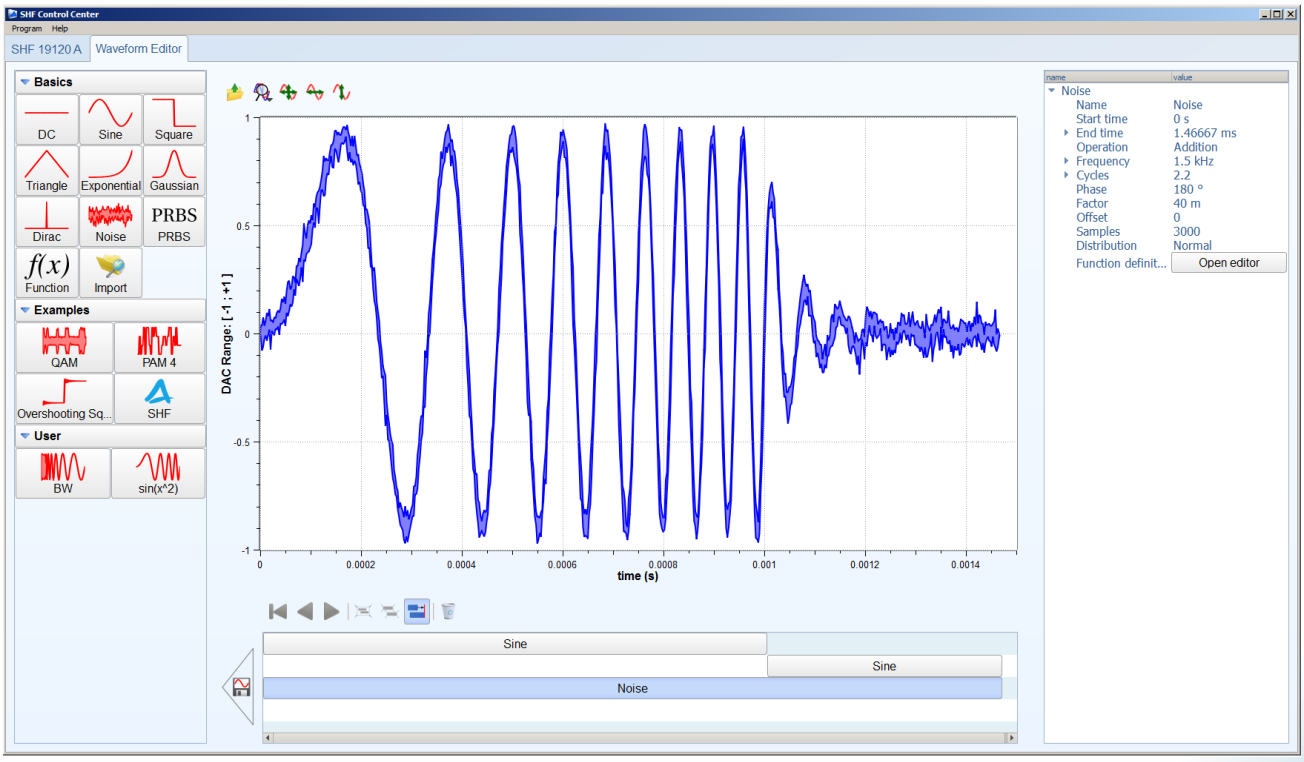
Software

The SHF 19120 C is operated via an Ethernet connection with the SHF Control Center software. An embedded version of the software comes pre-installed on the instrument which can be used without a PC, simply by connecting an HDMI monitor, a keyboard and a mouse (USB) to the rear panel.

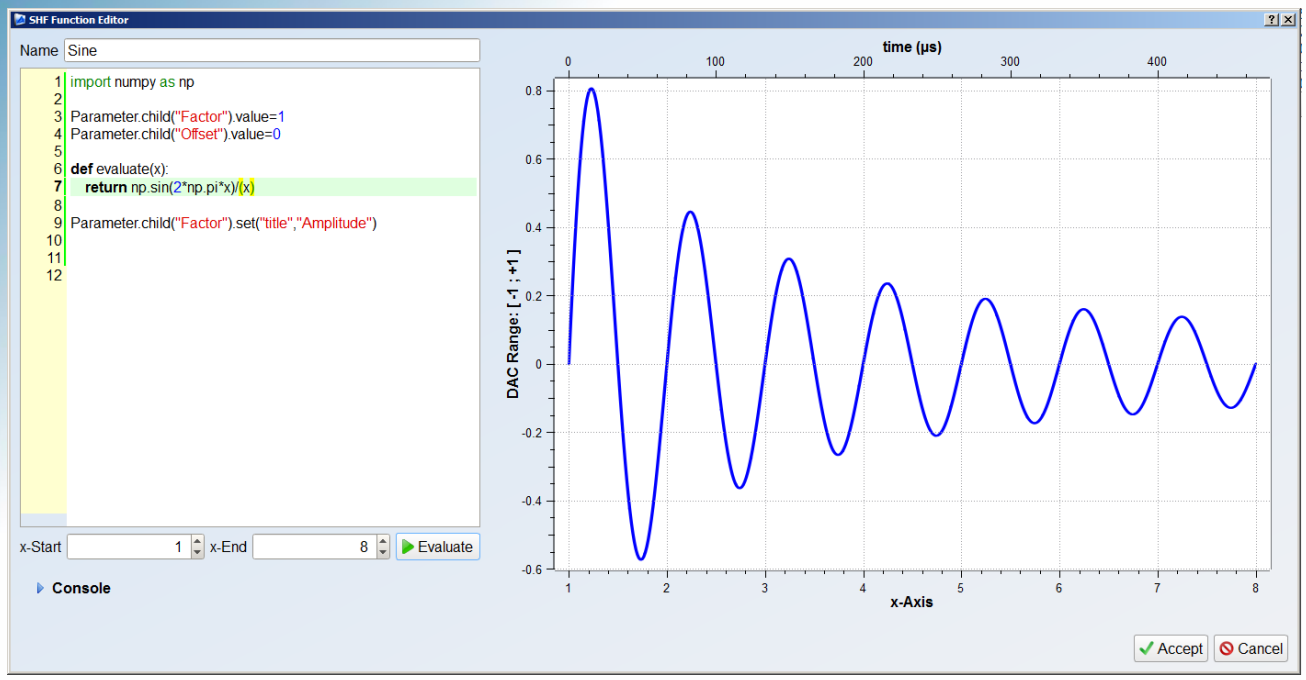


SHF Control Center Software

SHF Control Center Software: Trigger Settings and Waveform Library pop-up



SHF Control Center Software: Waveform Editor

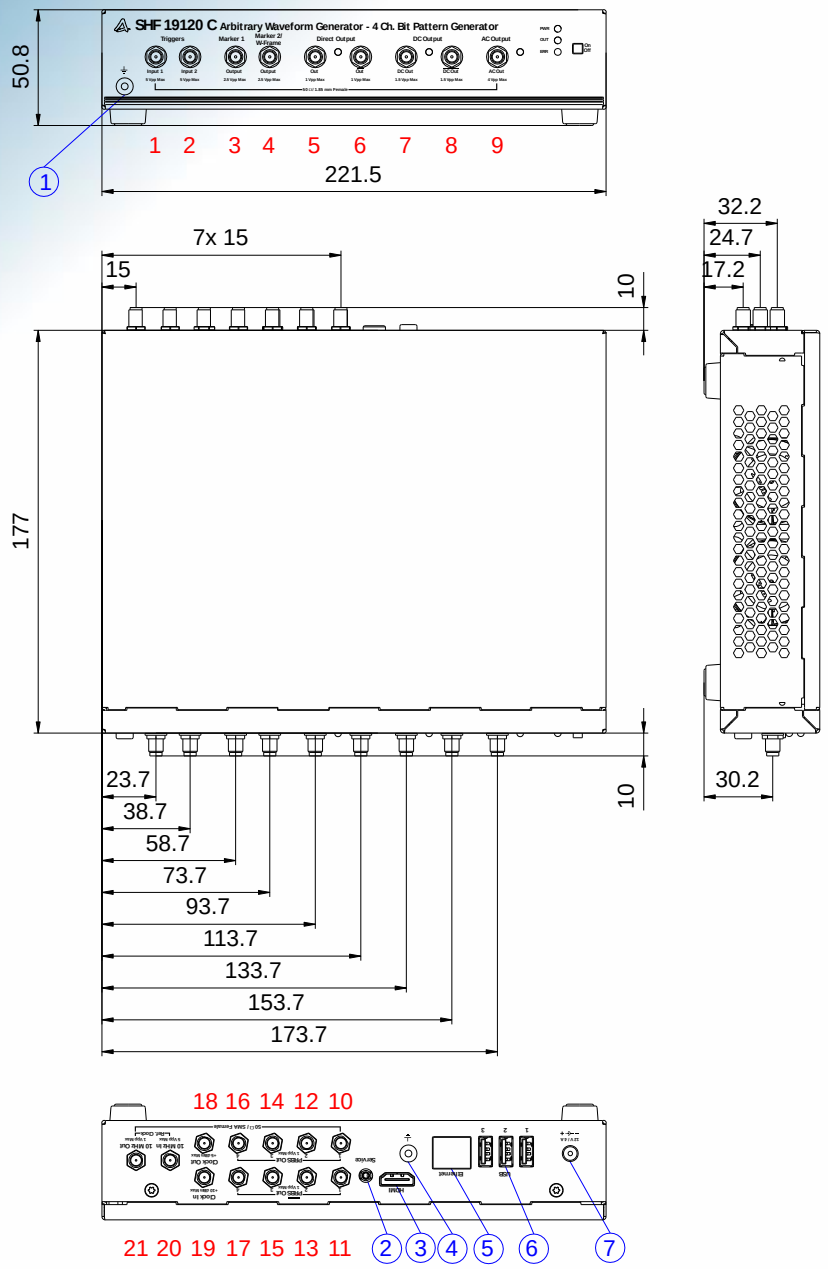


SHF Control Center Software: Python Equation Editor

	Channel 0	Channel 1	Channel 2	Channel 3
Bitrate	6.000 Gbps	6.000 Gbps	6.000 Gbps	6.000 Gbps
Type	PRBS 2^7-1	PRBS 2^{23}-1	PRBS 2^{31}-1	SQUARE2
Polarity	Non-Inverted	Non-Inverted	Non-Inverted	Non-Inverted
Delay	0 Bits	16 Bits	0 Bits	0 Bits
Amplitude	720 mV	720 mV	720 mV	720 mV
Pre-emphasis: Precursor	0 dB	0 dB	0 dB	0 dB
Pre-emphasis: Postcursor	0 dB	0 dB	0 dB	0 dB
Output	On	On	On	On

SHF Control Center Software: Detail of the Bit Pattern Generator Controls

Outline Drawing



Pos	Designation	Connector
1	Trigger Input 1	SMA
2	Trigger Input 2	SMA
3	Marker Output 1	SMA
4	Marker Output 2 / Word Frame Out	SMA
5	Direct Output Out	SMA
6	Direct Output $\overline{\text{Out}}$	SMA
7	DC Output DC Out	SMA
8	DC Output $\overline{\text{DC Out}}$	SMA
9	AC Output AC Out	SMA
10	PRBS 1	SMA
11	$\overline{\text{PRBS 1}}$	SMA
12	PRBS 2	SMA
13	$\overline{\text{PRBS 2}}$	SMA
14	PRBS 3	SMA
15	$\overline{\text{PRBS 3}}$	SMA
16	PRBS 4	SMA
17	$\overline{\text{PRBS 4}}$	SMA
18	Clock Out	SMA
19	Clock In	SMA
20	10MHz In	SMA
21	10MHz Out	SMA

Pos	Designation
1	GND
2	Service
3	HDMI
4	GND
5	Ethernet
6	USB
7	Power In

All dimensions are specified in millimeters (mm).