Quside

Product Datasheet

Quside Nellite™ FMC 400

The Quside Nellite™ FMC 400 is a **quantum entropy source** designed to provide a direct interface with FPGA-based moherboards and is compliant with the FPGA Mezzanine Card (FMC) ANSI/ VITA 57.1 2019 standard connector. The device operates at 400 Mb/s, with min-entropy bounds above 92%, and it is supplied with all the required firmware IP cores to operate, control, and interface the product.

Applications

Random numbers are required in a broad range of applications, including cybersecurity, high-performance computation, or gambling. The Quside Nellite™ FMC 400 is designed for high-performance quantum random generation for any FPGA product.

· Crypto-agile & quantum-safe deployments.

· Quantum key distribution

· Post-quantum cryptography

· Advanced entropy monitoring

· Cloud security

· Entropy-as-a-Service

· High-performance Monte Carlo simulations

· Synthetic data generation

Features

· 400 Mb/s raw generation rates.

· Above 90% quantum min-entropy bounds.

· Average min-entropy above 99%.

· Standard FMC interface (LPC/HPC) and FMC+.

· Designed for FPGA developers.

· VHDL IP cores supplied for module control, monitoring and randomness extraction. Compatible with Xilinx FPGAs series 7000 and UltraScale.

· Compliant with NIST SP800B recommendations and passes DieHarder and NIST SP800-22 test suites.

· Metrology and monitoring of the entropy source and entropy quality

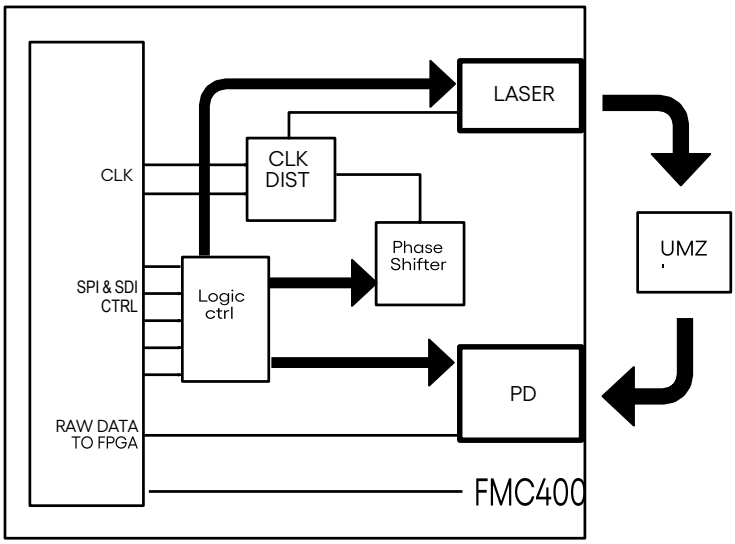


Figure 1. Block diagram of the Quside Nellite™ FMC 400.

Figure 1 shows a block diagram of the Quside Nellite™ FMC 400. The system consists of a randomness module card, hosting a laser, a photodetector, and an interferometer, all in a compact mechanical case. The randomness module card and interferometer are connected internally using polarization-maintaining fibers. The Quside Nellite™ FMC 400 card has an FMC port allowina a smooth connection to an FPGA baseboard.

ELECTRICAL SPECIFICATIONS

	Units	Min	Typ	Max
Power consumption	W		3.0	

Status monitor SPECIFICATIONS

	Units	Min	Typ	Max
Bias monitor	mA	38	40	43
Optical power monitor	dBm	-20		
Temperature monitor (T = environmental temp.)	°C			T + 20

RANDOMNESS SPECIFICATIONS

	Units	Min	Typ	Max
Quantum min-entropy[1]	Bits	0.9	0.93	
Raw bit rate	Mbps		400	
Extracted bit rate[2]	Mbps		290	

ABSOLUTE MAXIMUM RATINGS

	Units	Min	Typ	Max
Operating Temperature[3]	°C	20	25	70
Storage Temperature	°C	0	25	80

FPGA RESOURCE USAGE ESTIMATION

	LTU	F/F	DSP	BRAM 36/18
Control IP Core	5000	9000	0	8
Randomness extraction IP Core	2600	11000	260	8

[1] Average conditional min-entropy calculated as in C. Abellán et al., Phys. Rev. Lett. (2015) https://doi.org/10.1103/PhysRevLett.115.250403
[2] Extraction from 352 bits to 256 bits, using the randomness extractor from D. Frauchiger, R. Renner, & M. Troyer (2013), https://arxiv.org/abs/1311.4547
[3] Tested under the presented range.

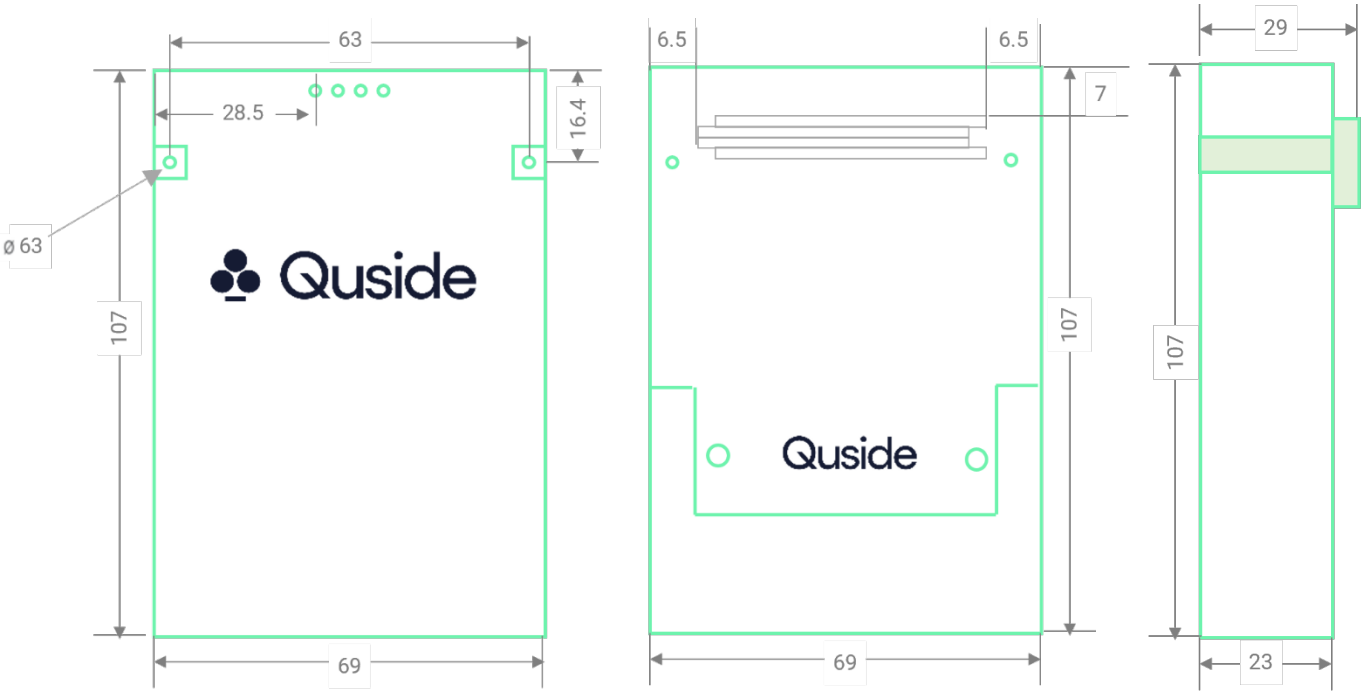
FMC PIN CONFIGURATION

FMC CONNECTOR: ASP-134488-01					
FMC Pin	FMC Net	NET Name	Type	Description	Level
C15	LA10_N	LED4	INPUT	LED	VADJ*
C19	LA14_N	LED3	INPUT	LED	VADJ*
C22	LA18_P_CC	LED2	INPUT	LED	VADJ*
C26	LA27_P	LED1	INPUT	LED	VADJ*
C30	SCL	IPMI_SCL	BI	I2C	3.3V
C31	SDA	IPMI_SDA	INPUT	I2C	3.3V
C34	GA0	GA0	INPUT	EEPROM Address. GA0 connected to EEPROM GA1 following ANSI.VITA57	3.3V
D08	LA01_P_CC	SPI_DIN	IN SPI	Output data	VADJ*
D35	GA1	GA1	INPUT	EEPROM Address. GA1 connected to EEPROM GA0 following ANSI.VITA57	3.3V
G06	LA00_P_CC	SPI_SYNC	IN GPIO	AD5061 SPI chip select	VADJ*
G07	LA00_N_CC	SPI_SCLK	IN SPI	AD5061 SPI Serial clock	VADJ*
G15	LA12_P	SDI_SCLK	IN SDI	NB6L295M serial clock	VADJ*
G16	LA12_N	SDI_SLOAD	IN SDI	NB6L295M serial load	VADJ*
G34	LA31_N	FMC400_REV	OUT GPIO	Pin to check revision of the FMC400. This pin is attached to GND in this rev.	GND
H04	CLK0_M2C_P	CLK_REC_P	OUTPUT	Clock recovery	LVDS
H05	CLK0_M2C_N	CLK_REC_N	OUTPUT	Clock recovery	LVDS
H07	LA02_P	RAW_FPGA_P	OUTPUT	Raw data output	LVDS
H08	LA02_N	PAW_FPGA_N	OUTPUT	Raw data output	LVDS
H16	LA11_P	SDI_SDIN	IN SDI	NB6L295M serial data in	VADJ*
H17	LA11_N	SDI_EN	IN SDI	NB6L295M enable	VADJ*
H31	LA28_P	CLK_SEL	OUT_GPIO	Switch select	VADJ*
H32	LA28_N	TX_DIS	IN GPIO	MAX3736 disable	VADJ*
H37	LA32_P	SCL	BI	I2C	VADJ*
H38	LA32_N	SDA	INPUT	I2C	VADJ*

Mechanical Specifications

The Quside Nellite™ FMC 400 optoelectronic parts are fully embedded in a compact mechanical case.

The module dimensions are 107 x 69 x 29 mm3, and two mounting holes are sized for an M2.5 screw.



Thanks for being part of our quantum journey!

To learn more about our products visit www.quside.com and contact: sales@quside.com